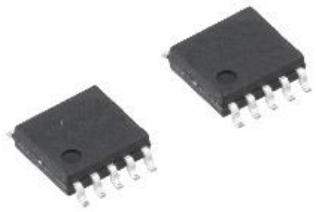
MITSUMI

AC-DC Flyback PWM Control IC with Built-in High Voltage Regulator

MM3665 Series



Overview

The MM3665 is the current mode flyback PWM control IC developed for quick charge adapters such as USB-PD.
The change in the auxiliary winding voltage of the transformer due to the change in the VBUS voltage of the USB-PD adapter is absorbed by the built-in regulator, and the power supply voltage is held constant. This doesn't require an external voltage regulator circuit.
In addition, you can correct and adjust the change of over current protective operation load current due to change of VBUS voltage by external resistor.
The IC can substantially reduce standby power by the start up circuit using the 740V high breakdown process and optimization of supply current. It operates PWM fixed frequency at heavy load, it operates bottom turn on by quasi resonant and the frequency is reduced by bottom skip at middle to light loads that minimizes power loss for each load condition and improves average efficiency.
Others, frequency jittering function, X capacitor discharge function make the measures of EMI easy. The IC which has various protection functions can assist safety design of power supply.

Features

- The primary side control IC suitable for variable output voltage power supplies such as USB-PD compatible AC adapters and printer power supplies
- 740V high breakdown voltage startup circuit reduces standby power
- No external regulator required due to built-in 140V breakdown voltage regulator
- Hybrid operation of fixed frequency and quasi-resonance achieves higher average efficiency and smaller transformer
- Built-in flexible over voltage protection function corresponded to output voltage
- Built-in over current protection function with flat characteristics regardless of AC input voltage
- The over current protection according to output voltage can be set by an external resistor
- Noise diffusion, downsize filter by frequency jitter function in all range
- X capacitor discharge function which don't increase standby power can make the measures of EMI easy
- Built-in AC input voltage brown-out function
- Built-in various protection functions and over temperature protection function

Main specifications

- HV Pin Input Voltage : 600V (Absolute max. 740V)
- AUXR Pin Input Voltage : 10V to 90V (Absolute max. 140V)
- Brown-In/Out Voltage : Typ. 72VAC/61VAC
- VDD Clamped Output Voltage : Typ. 12V
- Operating Current : Typ. 0.75mA in Latch 0.2mA
- Maximum Frequency : Typ. 66kHz

Packages

- SOP-10A

Application

- USB-PD Adaptor
- Quick charge Adaptor
- The variable output voltage power supply such as printer power supply

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Feb, 2022 Rev.0

Model Name

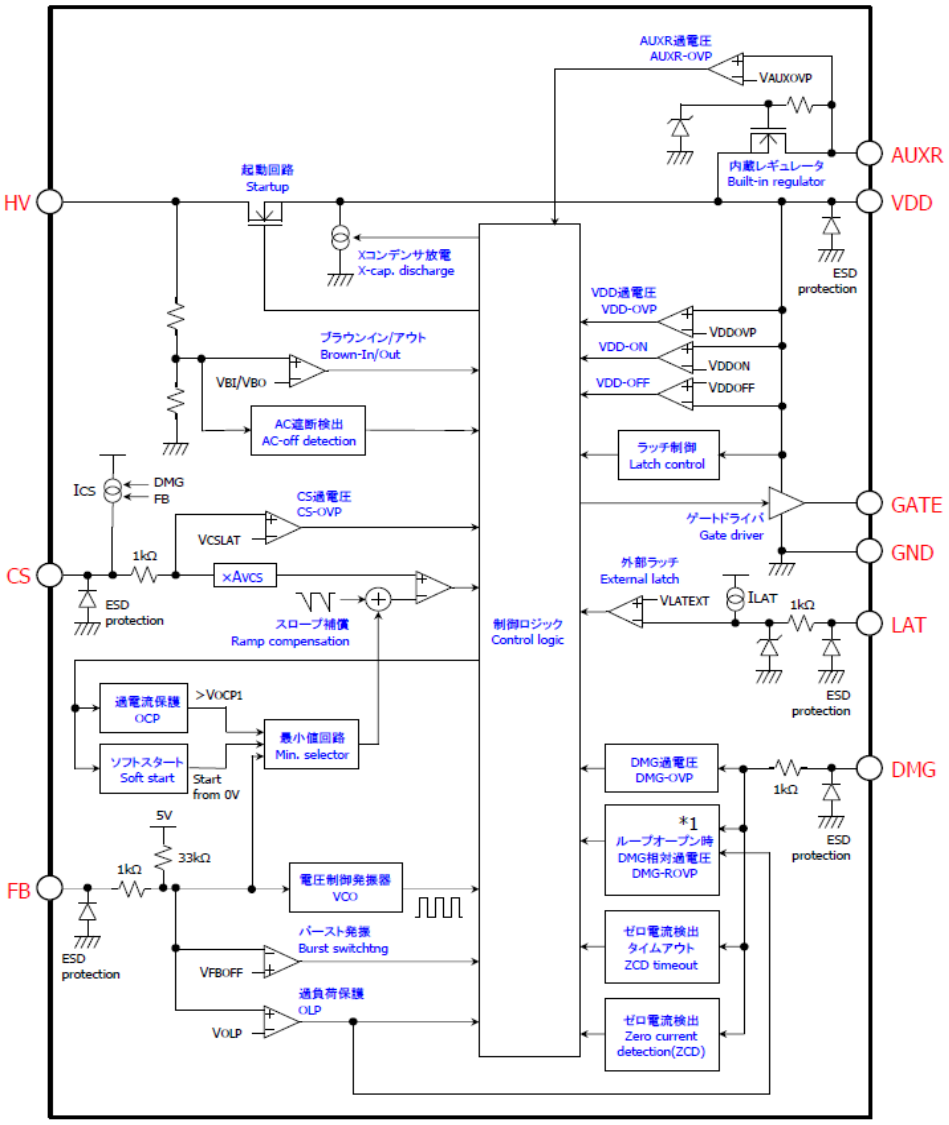
M M 3 6 6 5 X F F E H

Series Name (A) (B) (C) (D) (E)

(A)	
Function Type	
A	Auto restart type in OLP and ROVP
B	Latch type in OLP and ROVP
C	Auto restart type in OLP (ROVP is not equipped)
D	Latch type in over load protection OLP (ROVP is not equipped)

(B) Package : SOP-10A
(C) Type of Packing : F Housing
(D) Emboss Tape
(E) Halogen-free

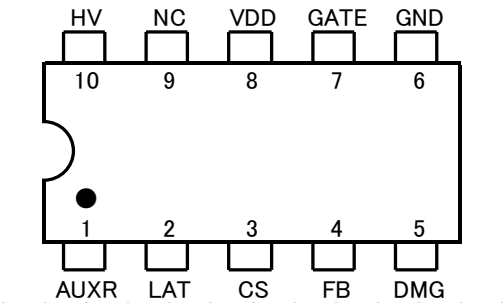
Block Diagram



Note:
*1 DMG-ROVP is A, B rank only

Pin Configuration

■ SOP-10A



端子 No.	端子名称	機能
1	AUXR	Built-in regulator input pin
2	LAT	External latch input pin
3	CS	Current sense pin
4	FB	Feedback input pin
5	DMG	Zero current detect pin
6	GND	Ground pin
7	GATE	Output pin
8	VDD	Power supply input pin
9	NC	No connection
10	HV	High voltage startup pin

Absolute Maximum Ratings

(T_A=25℃, unless otherwise specified)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Storage Temperature	T_{STG}	-40	150	℃
Operating Temperature	T_{OPR}	-40	125	℃
HV Pin Voltage	V_{HV}	-0.3	740	V
AUXR Pin Voltage	V_{AUXR}	-0.3	140	V
VDD Pin Voltage	V_{DD}	-0.3	34	V
LAT Pin Voltage	V_{LAT}	-0.3	5.5	V
CS Pin Voltage	V_{CS}	-0.3	5.5	V
FB Pin Voltage	V_{FB}	-0.3	5.5	V
DMG Pin Voltage *2	V_{DMG}	-	5.5	V
DMG Pin Current *2	$I_{DMGSOURCE}$	-2	-	mA
GATE Pin Voltage	V_{GATE}	-0.3	VDD	V
Gate Pin Peak Current	I_{OH}	-0.4	-	A
	I_{OL}	-	0.8	A
Power Dissipation (Alone)	P_{DIC}	-	350	mW
Power Dissipation (on PWB) *3	P_{DPWB}	-	890	mW

NOTES

*2 Negative voltage on DMG pin is clamped about -0.6V because of ESD protection diode.
To avoid large current of the diode, adjust external resistors.

*3 P_{DPWB} and θ_{JA} are influenced by design of PWB.
Power Dissipation (on PWB) is measured for the IC mounted on PWB :
57.3mm x 57.3mm, CEM-3, double layer,
thickness of the board = 1.0mm, Cu area ratio = 20%.
In this condition, thermal resistance from junction to ambient (θ_{JA}) is 140°C/W.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
HV Pin Input Voltage	V_{HVOP}	115	600	V
AUXR Pin Input Voltage	V_{AUXROP}	10	90	V
VDD Pin Input Voltage	V_{DDOP}	7.5	24	V
HV Pin Connection Resistance	R_{HV}	2.2	22	kΩ
X Capacitor Capacitance	C_X	0.1	5	uF
AUXR Pin Capacitance	C_{AUXR}	2.2	100	uF
VDD Pin Capacitance	C_{VDD}	0.47	100	uF
GATE Pin Load Capacitance	C_L	-	3000	pF
Operating Ambient Temperature	T_{OP}	-40	105	℃

Electrical Characteristics

(unless otherwise specified T_A=25°C, V_{HV}=120V, V_{DD}=V_{AUXR}=12V, V_{FB}=2V, V_{CS}=1V, V_{DMG}=1V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	*4
High Voltage Input Section (HV Pin)							
HV Input Current	I_{HVI}	In Operation V_{HV}=450V, V_{DD}=23V	10	16	27	uA	A
Startup HV Input Current	I_{HVSU}	In Startup V_{DD}=7V	4	6.1	9	mA	A
Brown-In Voltage	V_{BI}	V_{DD}=23V	91	101	111	V	A
Brown-Out Voltage	V_{BO}		76	86	96	V	A
Brown-Out Detection Hysteresis Voltage	V_{BOHYS}		-	15	-	V	A
Brown-Out Detection Delay Time	t_{BO}		40	60	80	ms	A
AC Off Detection Voltage Ratio	A_{ACOFF}	At peak of V_{HV}=175V	-	75	-	%	A
AC Off Detection Delay Time	t_{ACOFF}		20	30	40	ms	A
X-Capacitor Discharge Current	I_{XC}	V_{DD}=19V	1.4	-	-	mA	A
Power Supply Input Section (VDD Pin)							
Turn-On Operation Voltage	V_{DDON}		18.5	21	23.5	V	A
Turn-Off Operation Voltage	V_{DDOFF}		6	6.5	7	V	A
Operating Current	I_{DD1}	C_L=open	0.55	0.75	0.95	mA	A
Operating Current in No Switching	I_{DD2}	V_{FB}=0V	0.25	0.35	0.48	mA	A
Startup Charging Current	I_{CH}	V_{DD}=7V	-8.9	-5.9	-3.6	mA	A
Upper Limit Voltage in Latch	V_{DDLATU}	In latch	-	16	-	V	A
Lower Limit Voltage in Latch	V_{DDLATL}	In latch	-	11	-	V	A
Discharging Current in Latch	I_{DDLAT}	In latch, V_{DD}=13.5V	0.12	0.2	0.28	mA	A
Charging Current in Latch	I_{CHLAT}	In latch, V_{DD}=V_{DDLATL}	-8.9	-5.9	-3.6	mA	A
VDD Over Voltage Protection (OVP) Detection Voltage	V_{DDOVP}		25	27	29	V	A
VDD OVP Debounce Cycle *5	N_{VDDOVP}		-	4	-	cycle	-
Built-in Regulator Section (AUXR Pin, VDD Pin)							
VDD Clamped Output Voltage	V_{DDULIM}	V_{AUXR}=20V I_{DD}=-5mA	10	11.6	15.5	V	B
VDD Output Voltage	V_{DDOUT}	V_{AUXR}=10V I_{DD}=-1mA	7.3	7.8	9	V	B
AUXR Over Voltage Protection (OVP) Detection Voltage	$V_{AUXROVP}$		115	127	139	V	A
AUXR OVP Debounce Cycle *5	$N_{AUXROVP}$		-	4	-	cycle	-
Output Section (GATE Pin)							
Low Level Output Voltage	V_{OL}	I_{OL}=100mA	0.5	1.2	2.2	V	C
High Level Output Voltage	V_{OH}	I_{OH}=-20mA	9.4	10.4	11.4	V	C
Rise Time	t_{RISE}	C_L=1nF, V_{GATE}=10% to 90%	150	210	270	ns	D
Fall Time	t_{FALL}	C_L=1nF, V_{GATE}=90% to 10%	20	40	70	ns	D

Electrical Characteristics

(unless otherwise specified T_A=25°C, V_{HV}=120V, V_{DD}=V_{AUXR}=12V, V_{FB}=2V, V_{CS}=1V, V_{DMG}=1V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	*4
Oscillator Section							
Maximum Frequency	F_{MAX}	V_{FB}=2V	60	66	72	kHz	A
Minimum Frequency	F_{MIN}	V_{FB}=1V	20	22	24	kHz	A
VDD Coefficient of Frequency	A_{FVDD}	V_{DD}=10V to 24V	-2	-	2	%	A
Temperature Coefficient of Frequency*5	A_{FTEMP}	T_A=-40°C to 125 °C	-5	-	5	%	-
Frequency Jitter Ratio	A_{FJR}	V_{FB}=2V	±3	±5.5	±8	%	A
Maximum On Duty Cycle	D_{MAX}	V_{CS}=0V	75	84	91	%	A
Feedback Section (FB Pin)							
FB Source Current	I_{FB}	V_{FB}=0V	-200	-150	-100	uA	A
Turn-Off Switching Voltage	V_{FBOFF}		0.42	0.5	0.58	V	A
Turn-Off Switching Hysteresis Voltage	V_{FBHYS}		-	0.06	-	V	A
Decrease in Frequency Entry Voltage	$V_{FBENTRY}$	freq < F_{MAX} × 0.99	1.58	1.64	1.7	V	A
Decrease in Frequency End Voltage	V_{FBEND}	freq > F_{MIN} × 1.01	1.13	1.19	1.25	V	A
Over Load Protection (OLP) Detection Voltage	V_{OLP}		3.5	4	4.5	V	A
OLP Delay Time	t_{OLP}		190	250	310	ms	A
Auto Restart Time	t_{ARS}	A,C rank only	1.5	2	2.5	s	A
Current Sense Section (CS Pin)							
Voltage Gain	A_{VCS}		-	4.8	-	V/V	A
GATE Turn-Off Delay Time *5	t_{OFF}		-	200	-	ns	-
Minimum On Time 1	t_{MIN1}	After soft start and V_{FB} < V_{OLP}	400	600	800	ns	A
Minimum On Time 2	t_{MIN2}	In soft start or V_{FB} > V_{OLP}	200	300	400	ns	A
Soft Start Time *5	t_{SS}		-	4.8	-	ms	-
OCP Detection Voltage 1	V_{OCP1}	duty=0%	0.355	0.375	0.395	V	A
OCP Detection Voltage 2	V_{OCP2}	duty=45%	0.605	0.640	0.675	V	A
CS Latch-Off Voltage	V_{CSLAT}		1.1	1.2	1.3	V	A
CS Latch-Off Debounce Cycle*5	N_{CSLAT}		-	4	-	cycle	-
CS Source Current 1	I_{CS1}	V_{DMG}=0.7V, V_{FB}=3V	-55	-45	-35	uA	A
CS Source Current 2	I_{CS2}	V_{DMG}=2.9V, V_{FB}=3V	-	-0.8	-	uA	A

Electrical Characteristics

(unless otherwise specified T_A=25°C, V_{HV}=120V, V_{DD}=V_{AUXR}=12V, V_{FB}=2V, V_{CS}=1V, V_{DMG}=1V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	*4
Zero Current, Secondary Voltage Detection Section (DMG Pin)							
Zero Current Detection (ZCD) Voltage	V_{ZCD}		40	90	150	mV	A
ZCD Hysteresis Voltage	V_{ZCDHYS}		-	80	-	mV	A
GATE Turn-On Delay Time *5	t_{ON}		-	240	-	ns	-
ZCD Time-Out Entry Voltage	V_{TO}		0.4	0.5	0.6	V	A
ZCD Time-Out Hysteresis Voltage	V_{TOHYS}		-	0.1	-	V	A
ZCD Time-Out	t_{TO}		5.5	8.5	11.5	us	A
DMG Constant OVP Detection Voltage	V_{DMGOVP}		3.2	3.4	3.6	V	A
DMG OVP Detection Blanking Time	$t_{DMGBLANK}$	FB=2V	1.9	2.7	3.5	us	A
DMG OVP Debounce Cycle *5	N_{DMGOVP}		-	4	-	cycle	-
DMG ROVP at Open Loop	ΔV_{ROVP}	*6 A,B rank only	0.3	0.375	0.45	V	A
DMG ROVP Upper Limit at Open Loop	$V_{ROVPMAX}$	*7 A,B rank only	2.8	3	3.2	V	A
DMG ROVP Lower Limit at Open Loop	$V_{ROVPMIN}$	*8 A,B rank only	1.15	1.3	1.45	V	A
DMG ROVP Debounce Cycle at Open Loop *5	N_{ROVP}	A,B rank only	-	4	-	cycle	-
External Latch Section (LAT Pin)							
LAT Source Current	I_{LAT}		-36	-32	-28	uA	A
External Latch-Off Voltage	V_{LATEXT}		0.32	0.36	0.4	V	A
External Latch-Off Debounce Cycle *5	N_{LATEXT}		-	4	-	cycle	-
LAT Pin Open Voltage	$V_{LATOPEN}$	LAT=open	-	1.8	-	V	E
Internal Temperture Protection Section							
Over Temperture Protection (OTP) Threshold *5	T_{OTP}		-	150	-	°C	-
OTP Debounce Cycle *5	N_{OTP}		-	4	-	cycle	-

NOTES

*4 Symbols for the test circuits.

*5 Guaranteed by design

*6 Tested with the following steps (a) to (d).

(a) $V_{FB} < V_{OLP}$, V_{DMG} = 1.8V

(b) $V_{FB} > V_{OLP}$

(c) Increase VDMG

(d) For VDMG where stopped switching, $\Delta V_{ROVP} = V_{DMG} - 1.8V$

*7 Tested with the following steps (a) to (d).

(a) $V_{FB} < V_{OLP}$, V_{DMG} = 2.8V

(b) $V_{FB} > V_{OLP}$

(c) Increase VDMG

(d) For VDMG where stopped switching, $V_{ROVPMAX} = V_{DMG}$

*8 Tested with the following steps (a) to (d).

(a) $V_{FB} < V_{OLP}$, V_{DMG} = 0V

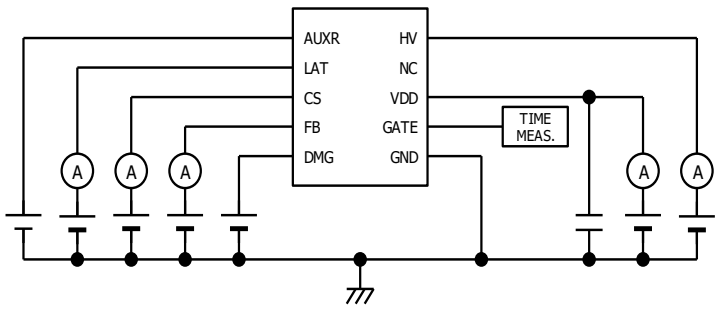
(b) $V_{FB} > V_{OLP}$

(c) Increase VDMG

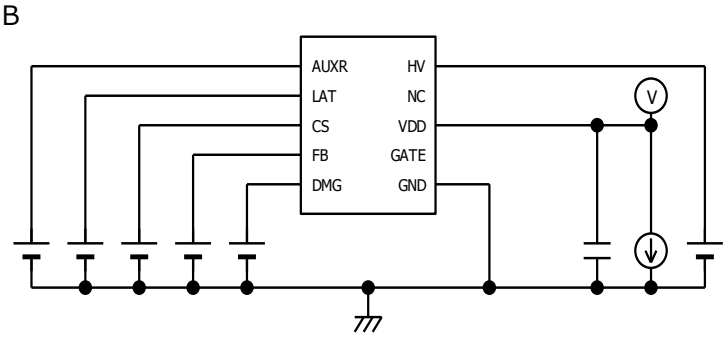
(d) For VDMG where stopped switching, $V_{ROVPMIN} = V_{DMG}$

Test Circuits

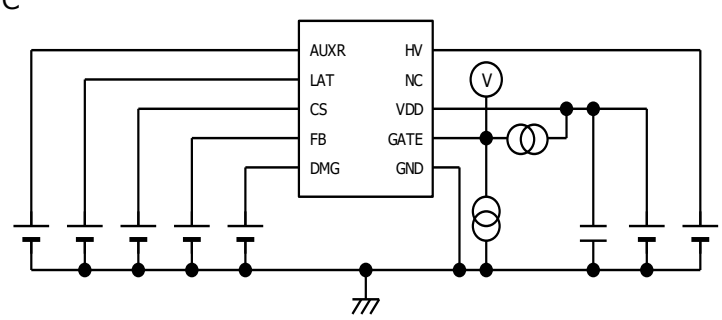
TEST CIRCUIT A



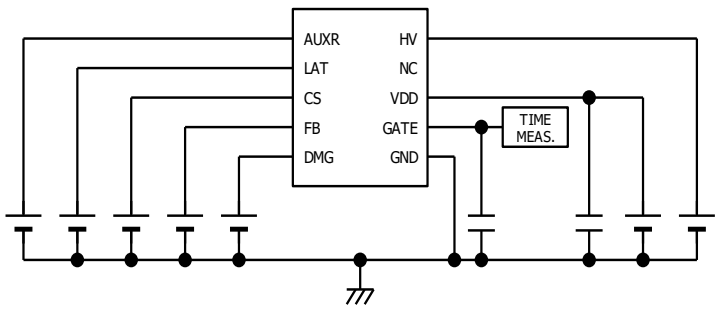
TEST CIRCUIT B



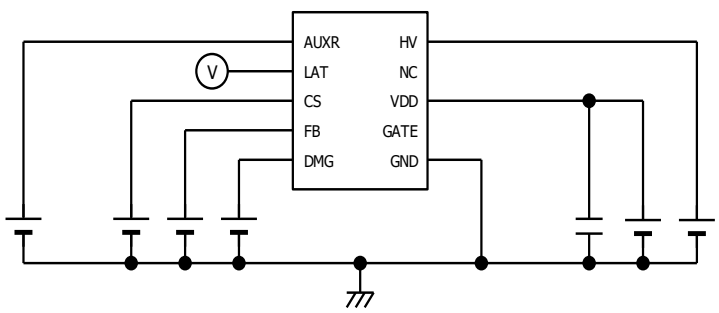
TEST CIRCUIT C



TEST CIRCUIT D

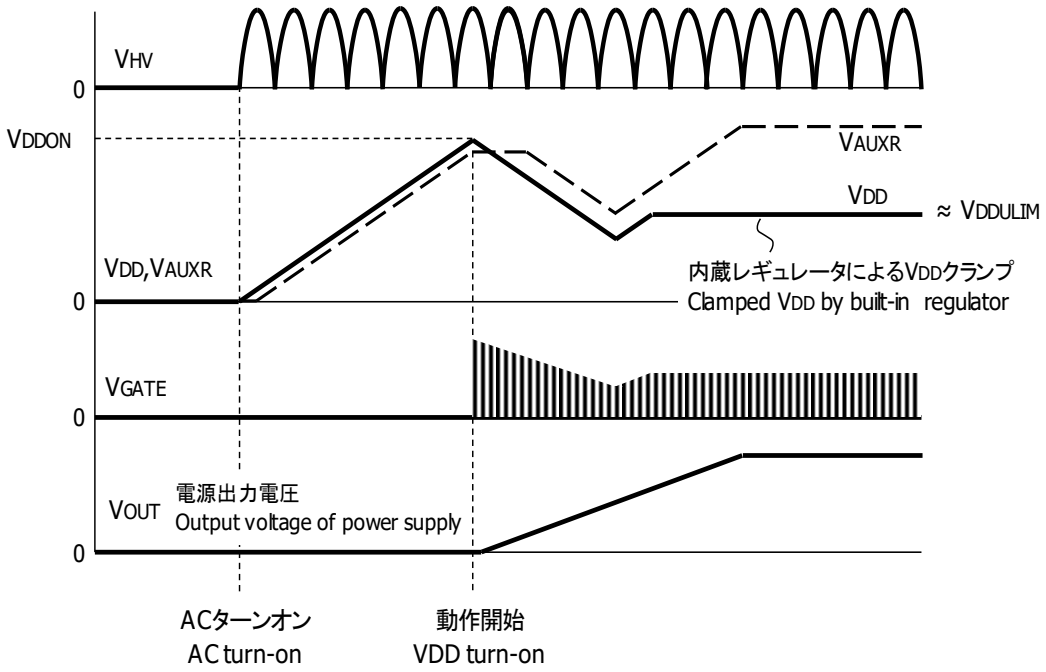


TEST CIRCUIT E

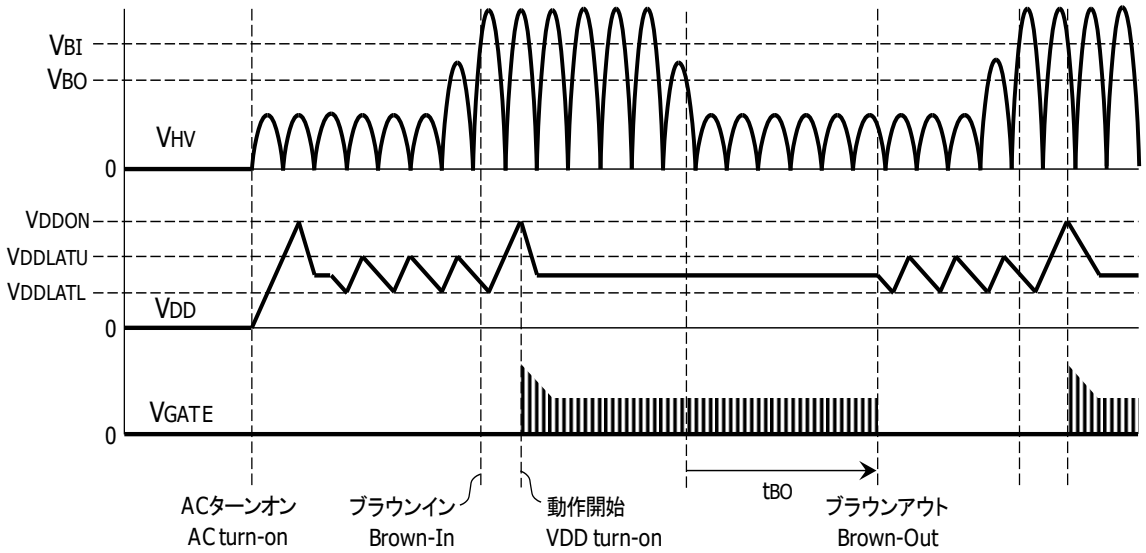


Timing Chart

Start up

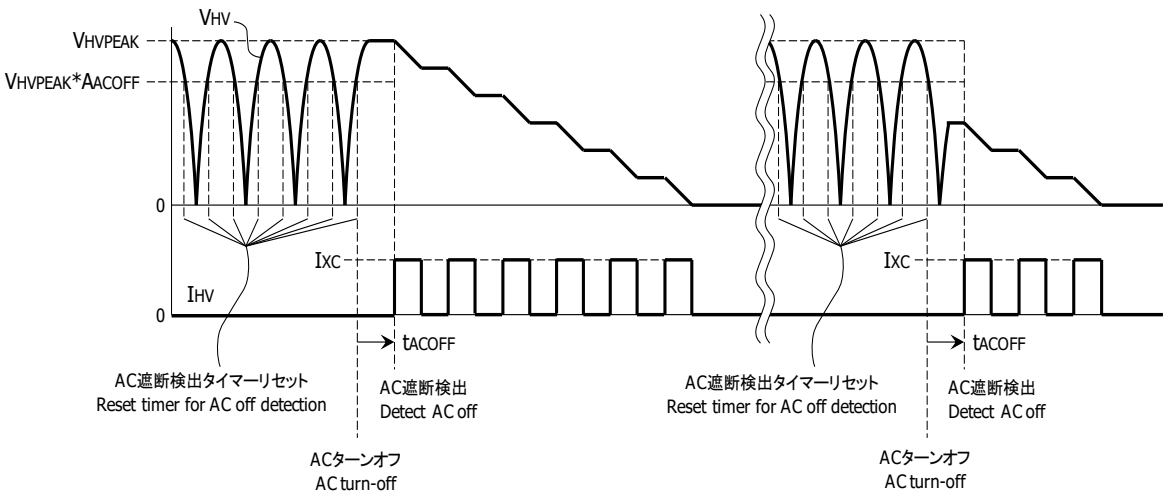


Brown-In, Brown-Out

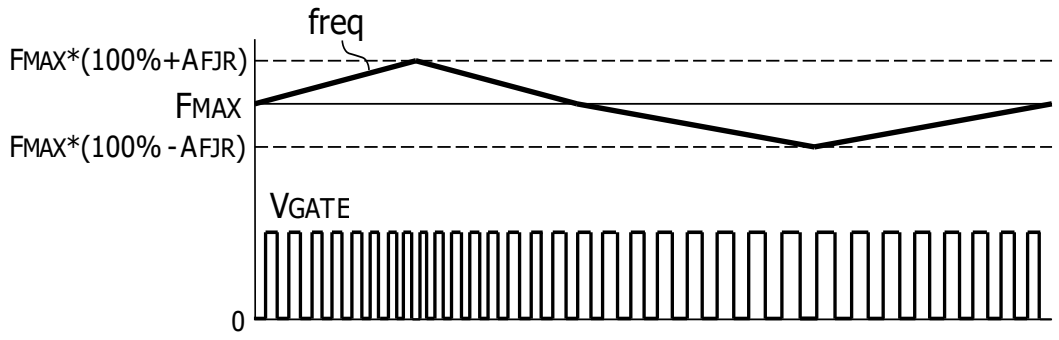


Timing Chart

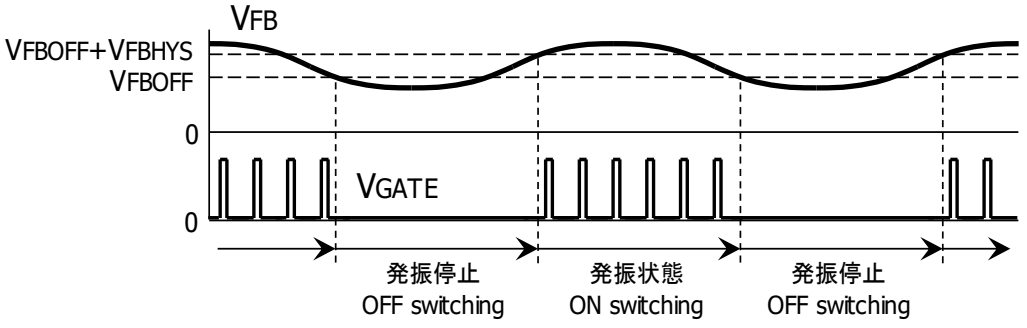
X-Cap. Discharge



Frequency Jitter

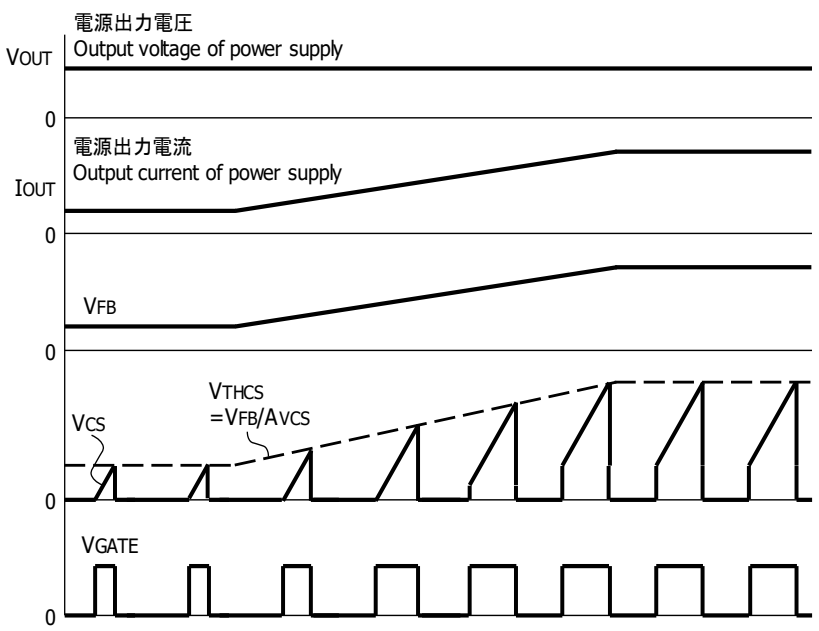


Burst Switching

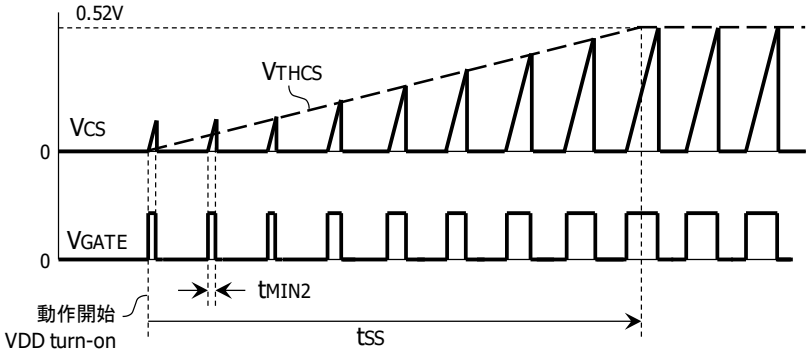


Timing Chart

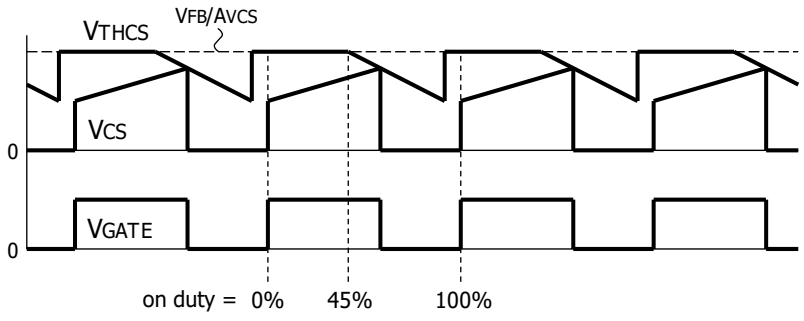
Current Mode Control



Soft Start

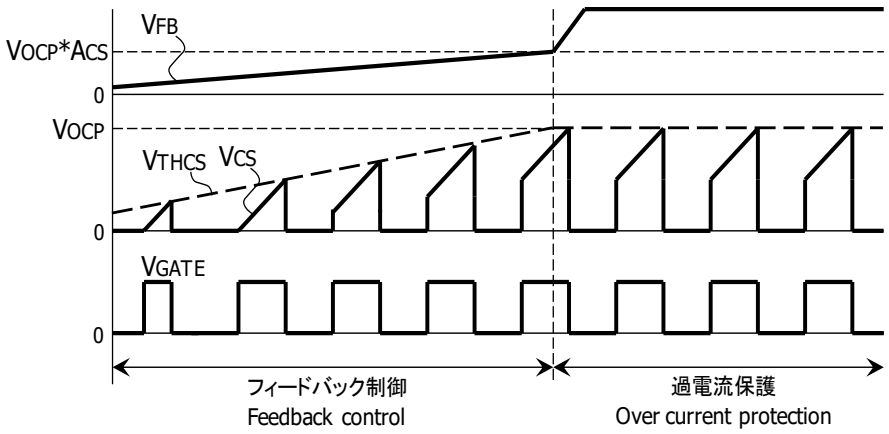


Ramp Compensation

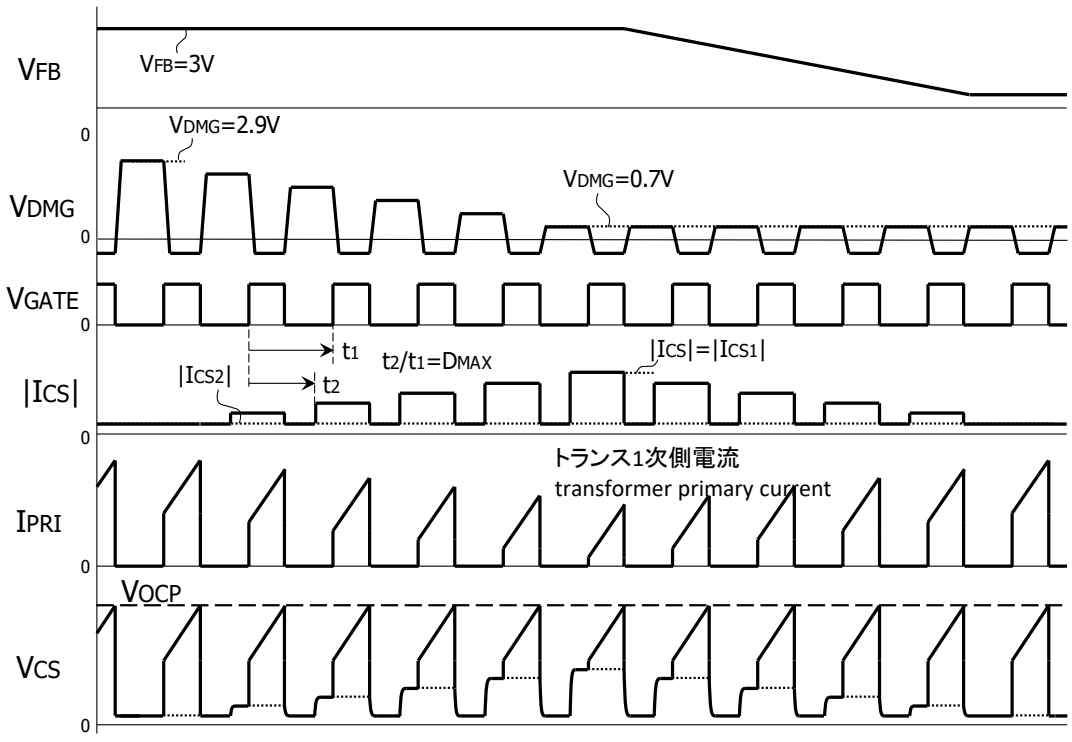


Timing Chart

Over Current Protection (OCP)

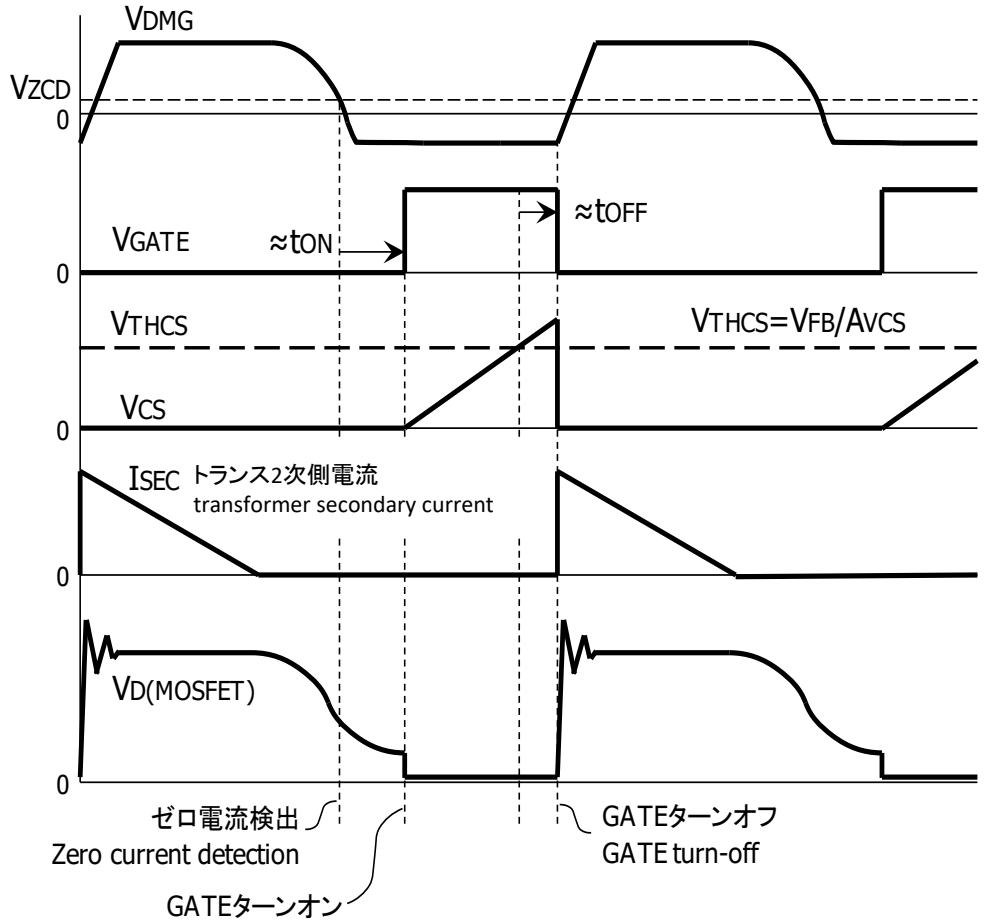


OCP Compensation Linked Output Voltage

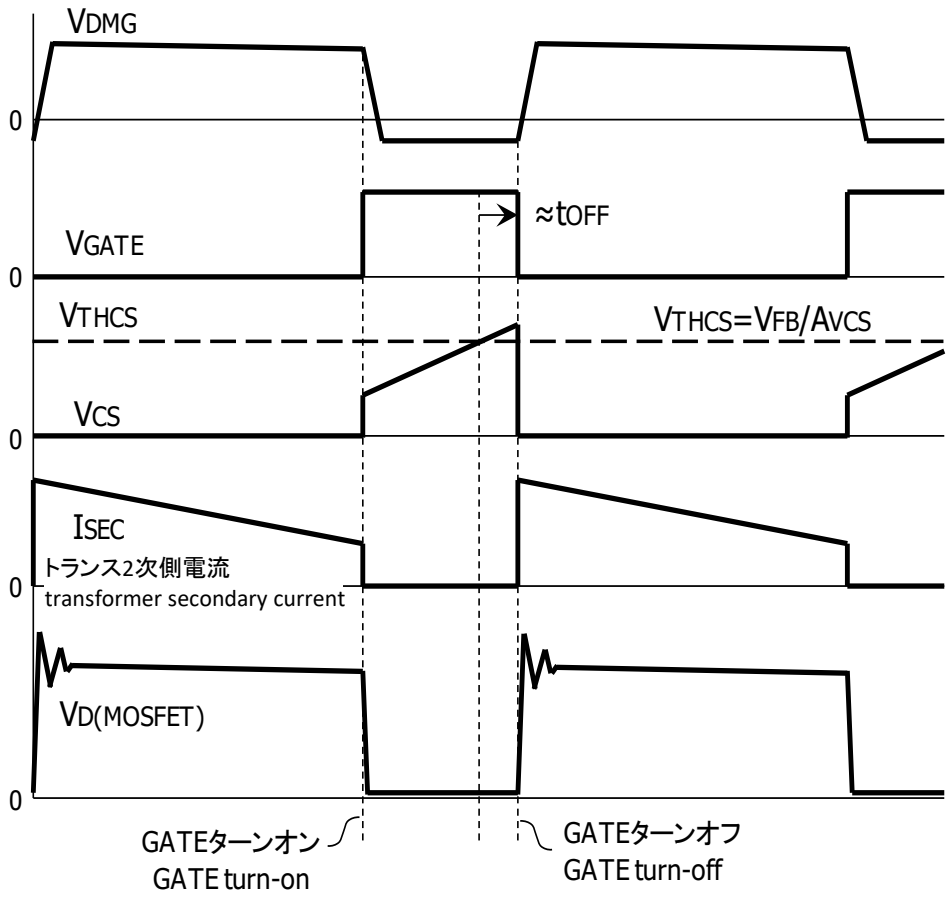


Timing Chart

Quasi-Resonance Mode

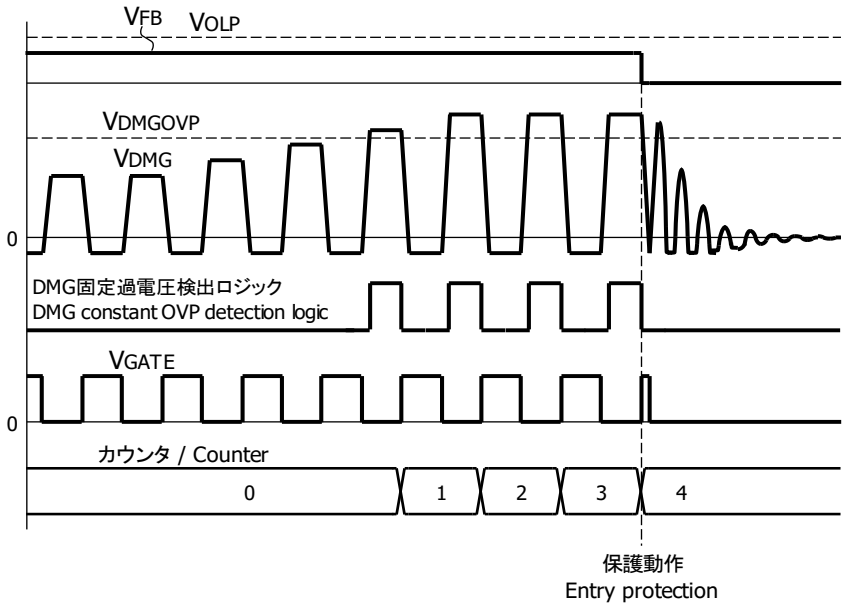


Continuous Current Mode

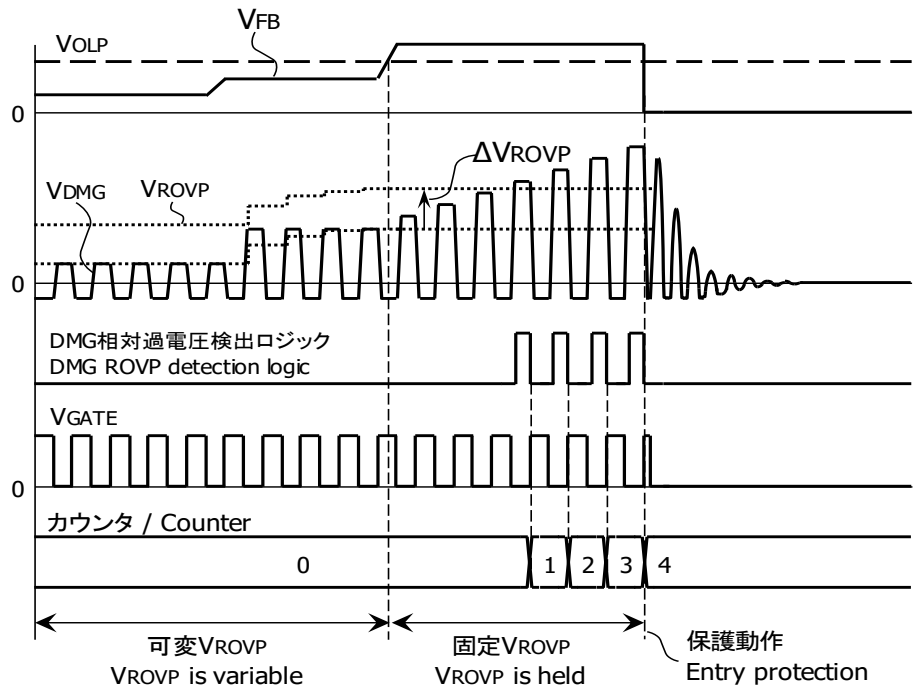


Timing Chart

DMG Constant Over Voltage Protection (OVP)



DMG Relative Over Voltage Protection (ROVP)



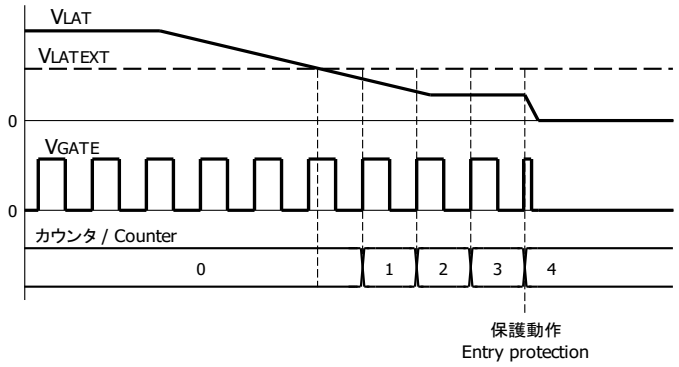
When $V_{ROVP}<V_{ROVPMIN}$, protection threshold voltage is clamped to $V_{ROVPMIN}$.

When $V_{ROVP}>V_{ROVPMAX}$, protection threshold voltage is clamped to $V_{ROVPMAX}$.

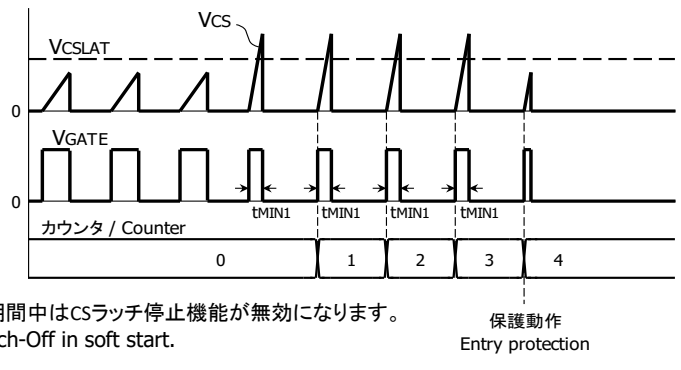
In soft start, V_{ROVP} is not held.

Timing Chart

External Latch

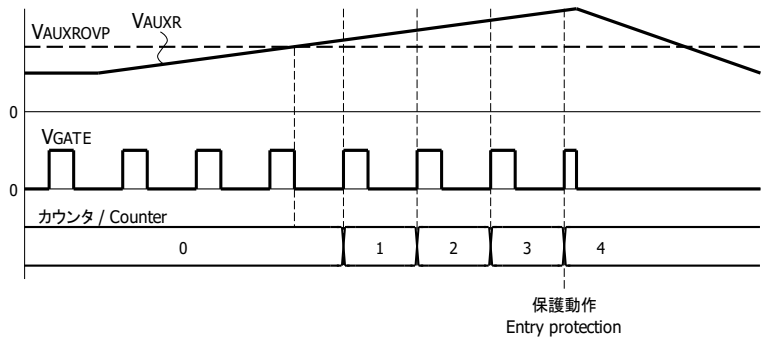


CS Latch-Off

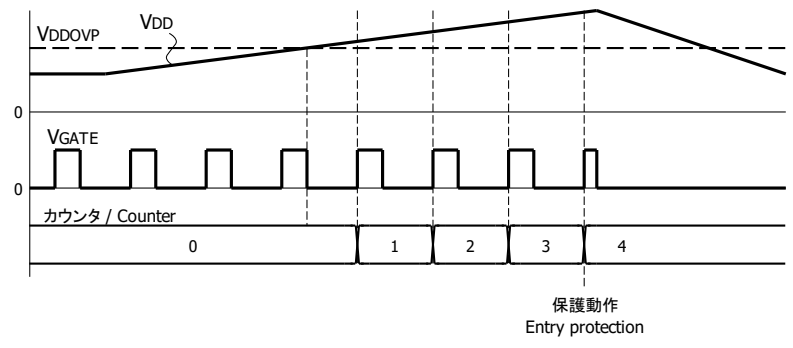


ソフトスタート期間中はCSラッチ停止機能が無効になります。
Invalid CS Latch-Off in soft start.

AUXR OVP

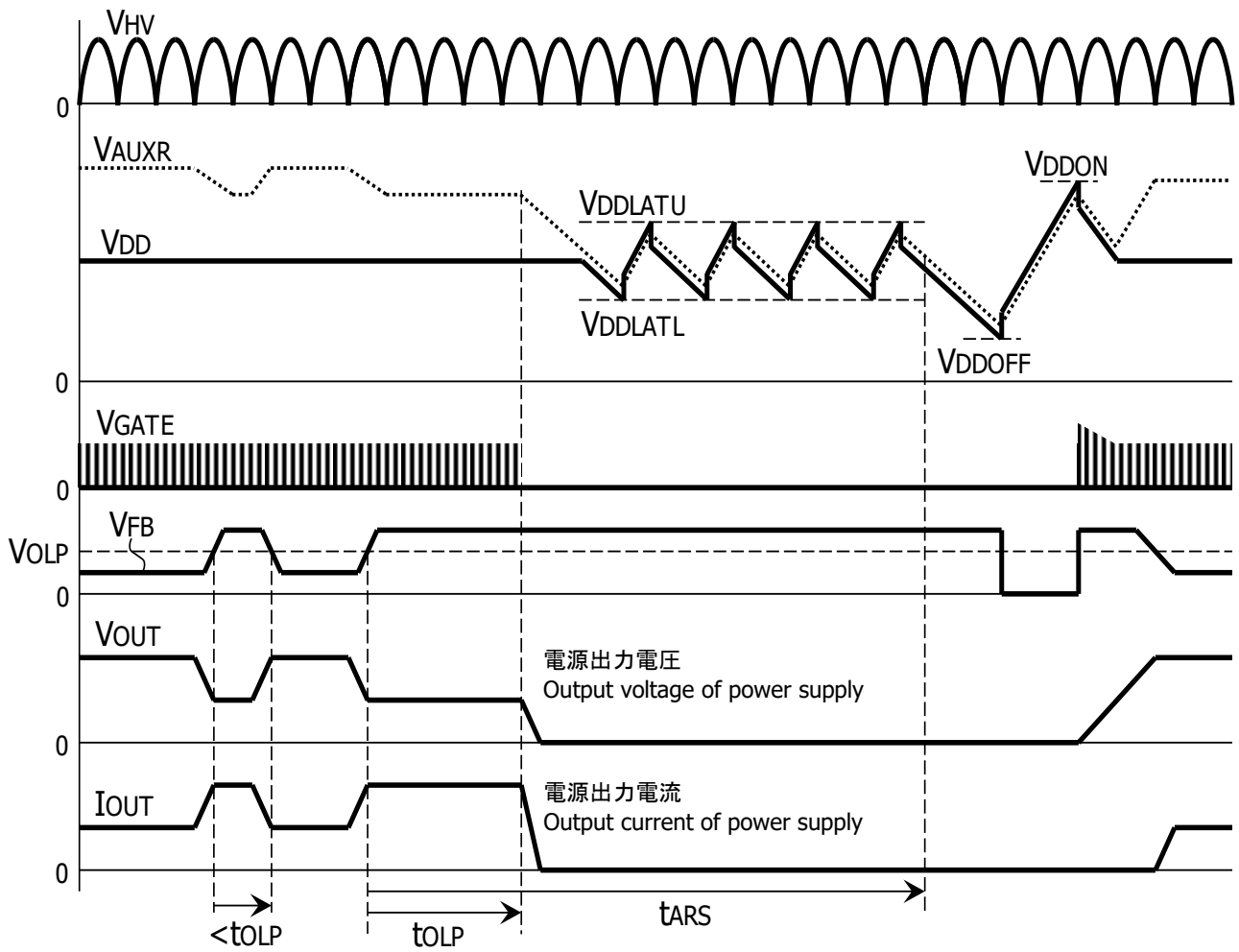


VDD OVP

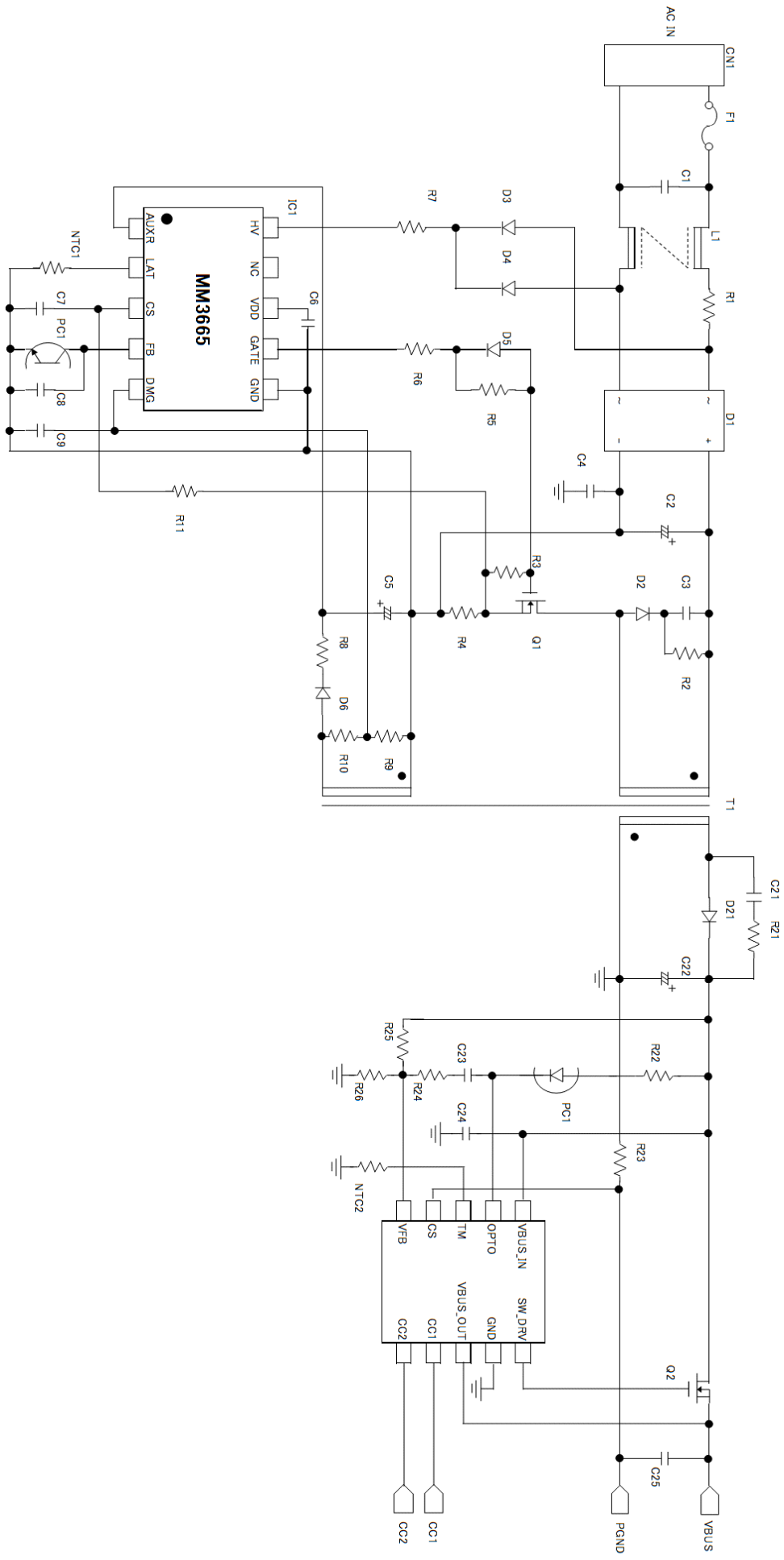


Timing Chart

Over Load Protection and Auto Restart (A,C rank only)



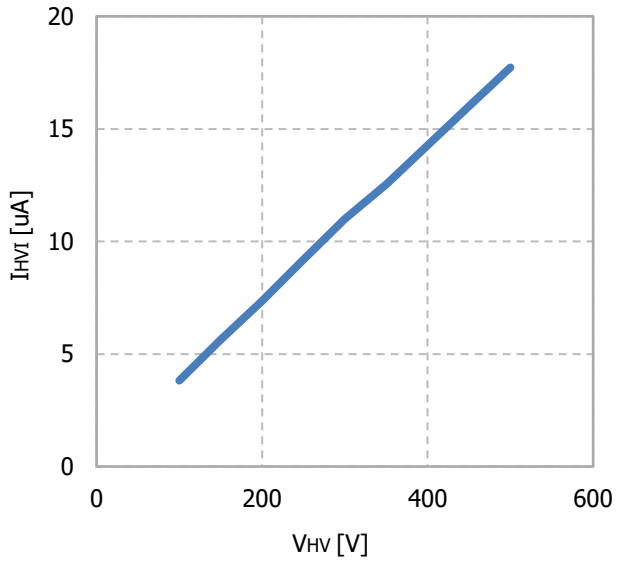
Typical Application Circuit



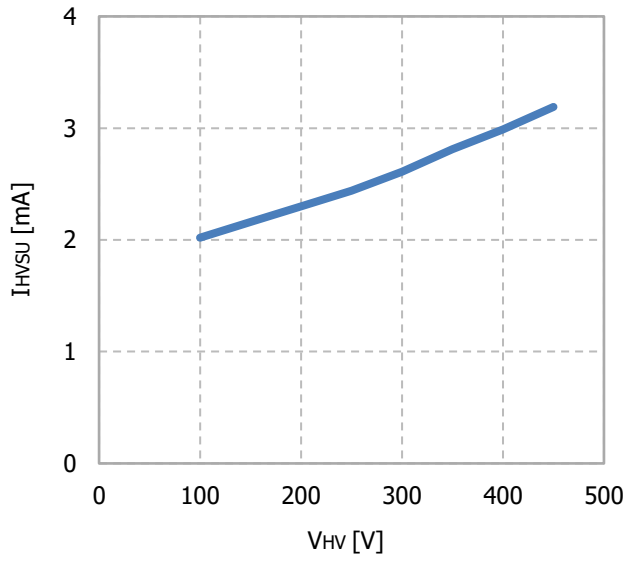
Typical Performance Characteristics

(unless otherwise specified TA=25℃)

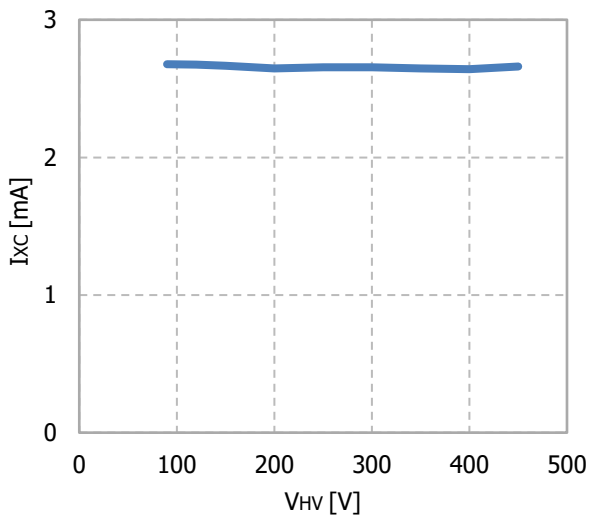
VHV vs. HV Input Current



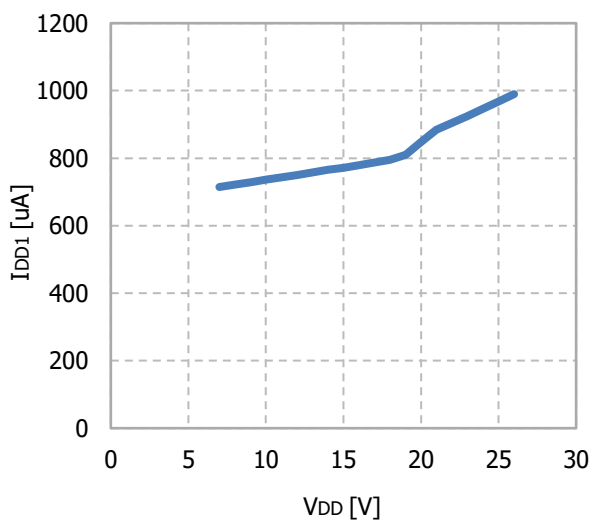
VHV vs. Startup HV Input Current (VDD=20V)



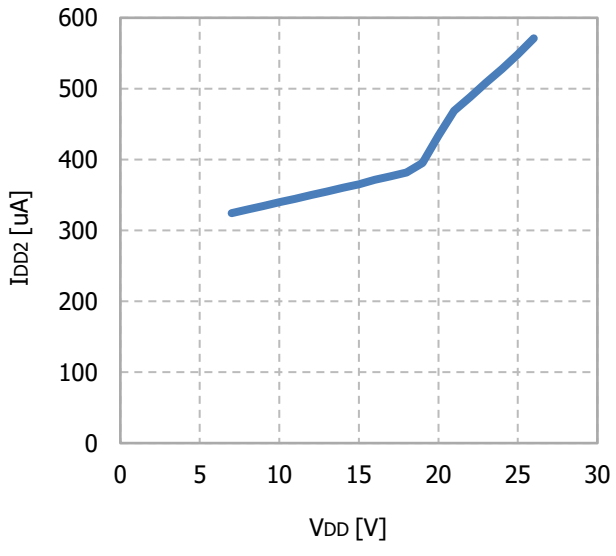
VHV vs. X-Capacitor Discharge Current



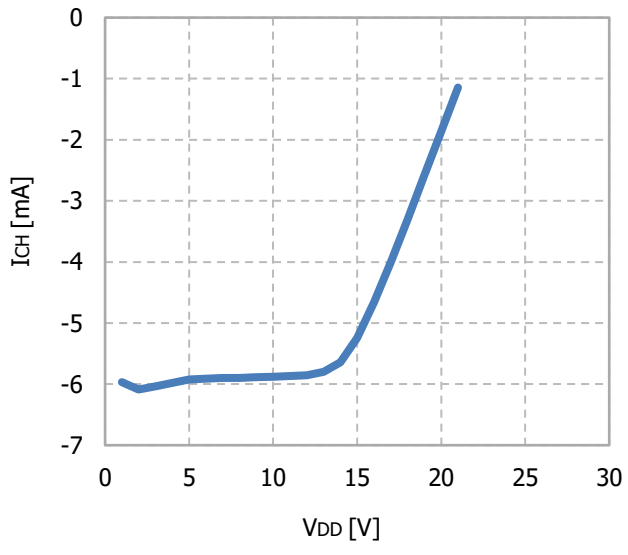
VDD vs. Operating Current



VDD vs. Operating Current in No Switching



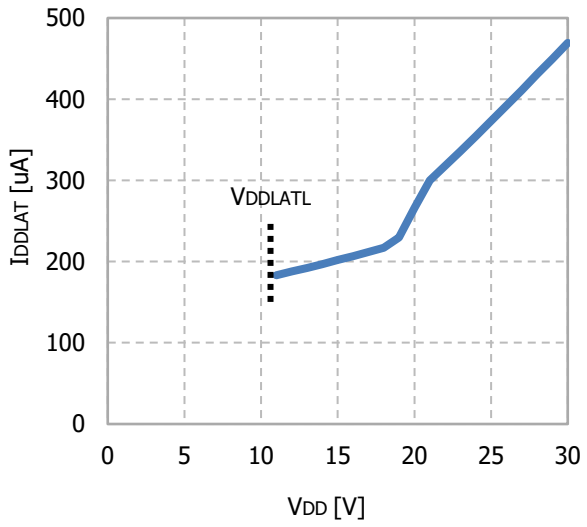
VDD vs. Startup Charging Current



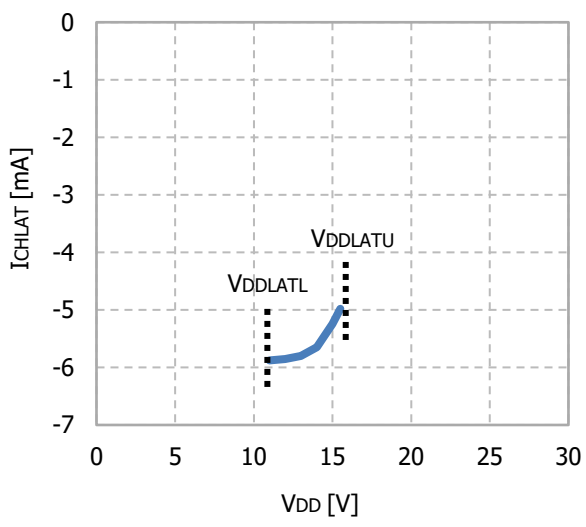
Typical Performance Characteristics

(unless otherwise specified TA=25℃)

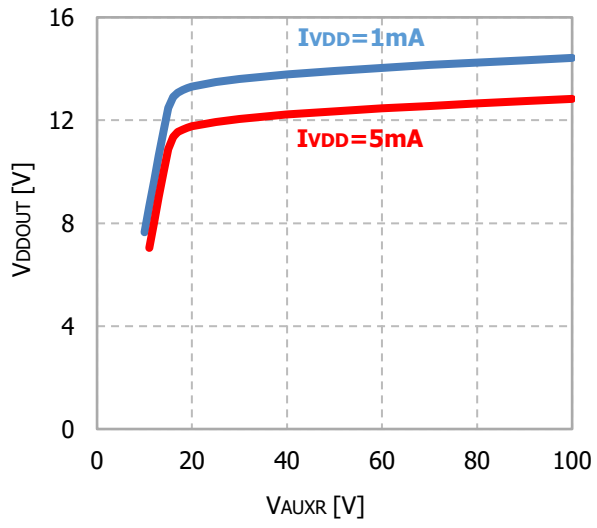
VDD vs. Discharging Current in Latch



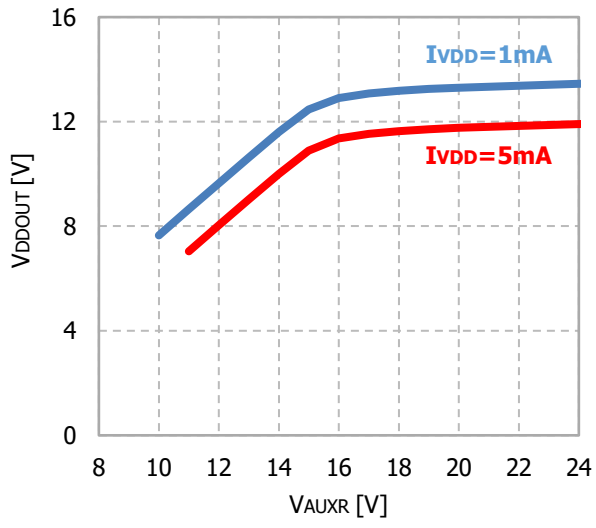
VDD vs. Charging Current in Latch



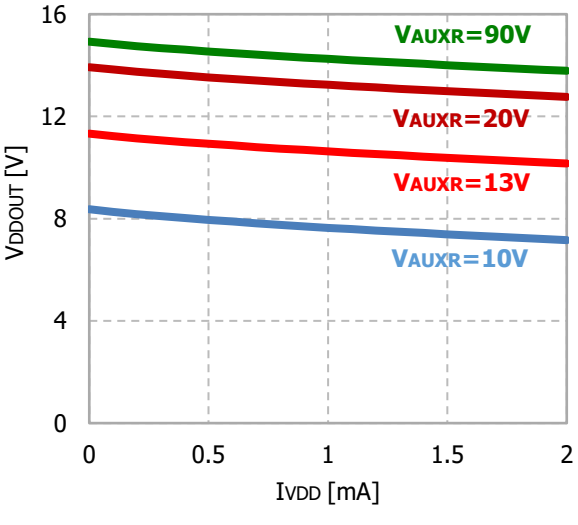
Line Regulation of Built-in Regulator (10V to 100V)



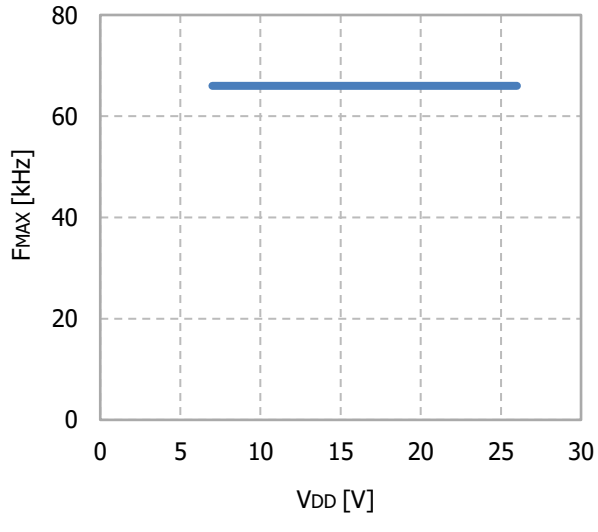
Line Regulation of Built-in Regulator (10V to 24V)



Load Regulation of Built-in Regulator



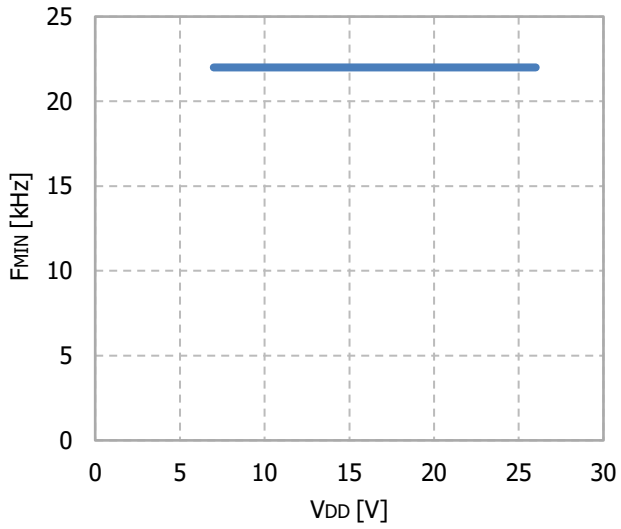
VDD vs. Maximum Frequency



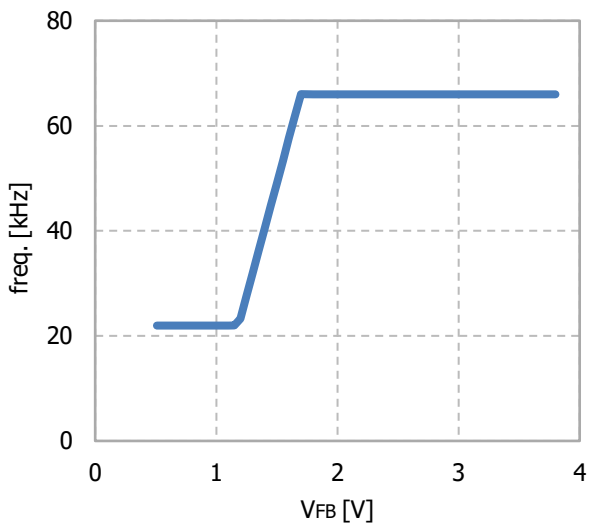
Typical Performance Characteristics

(unless otherwise specified TA=25℃)

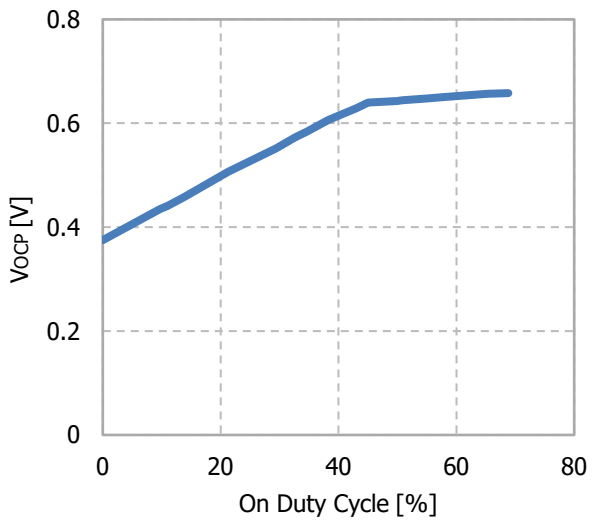
VDD vs. Minimum Frequency



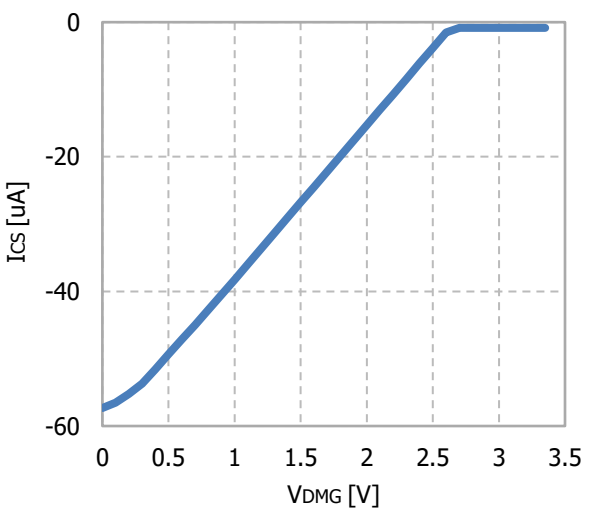
VFB vs. Switching Frequency



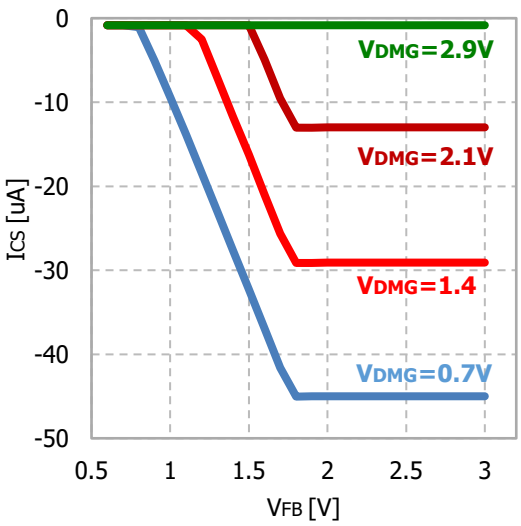
On Duty Cycle vs. OCP Detection Voltage



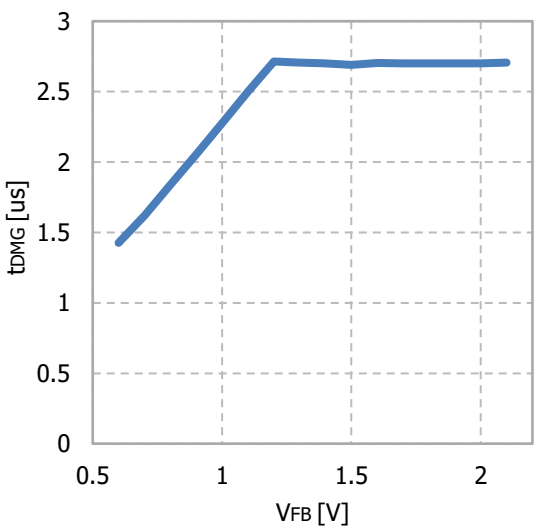
VDMG vs. CS Source Current



VFB vs. CS Source Current



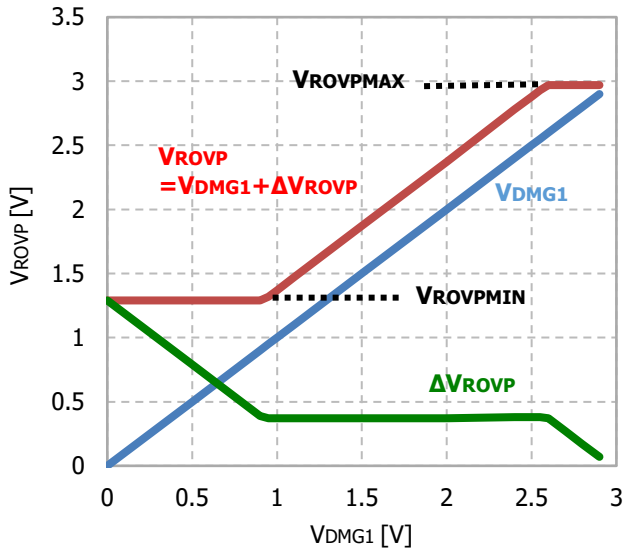
VFB vs. DMG OVP Detection Blanking Time



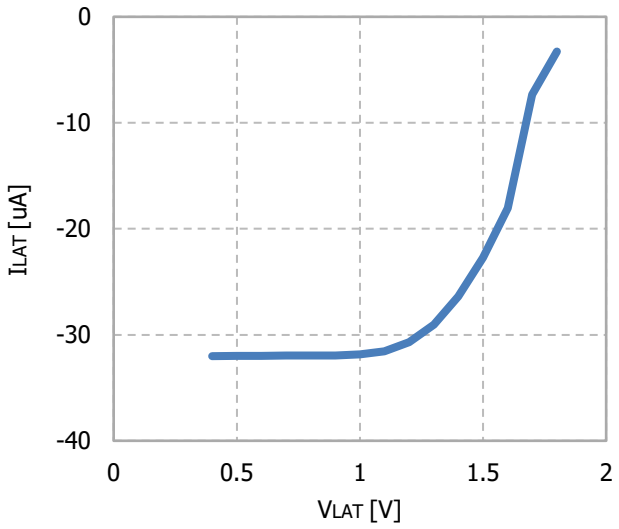
Typical Performance Characteristics

(unless otherwise specified TA=25℃)

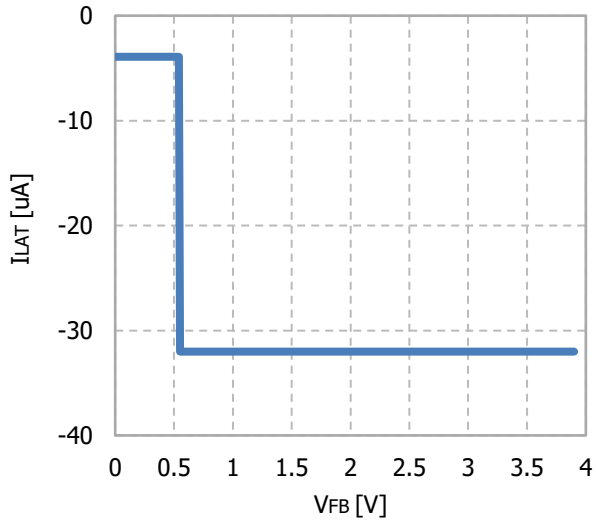
VDMG Before Open Loop (VDMG1) vs. DMG Relative Over Voltage Protection Detection Voltage (VROVP)



VLAT vs. LAT Source Current

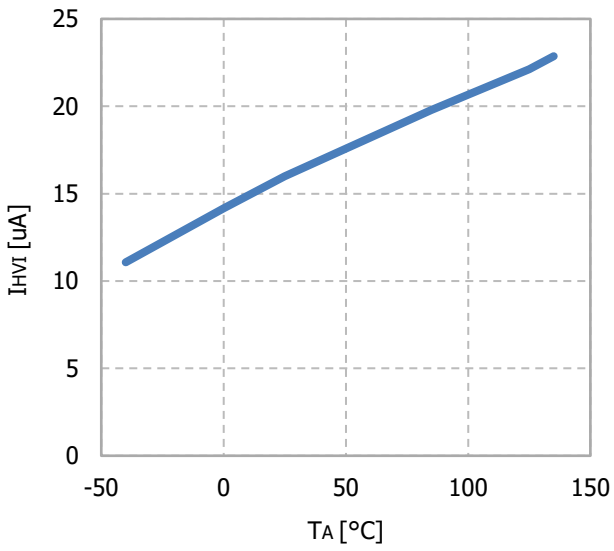


VFB vs. LAT Source Current

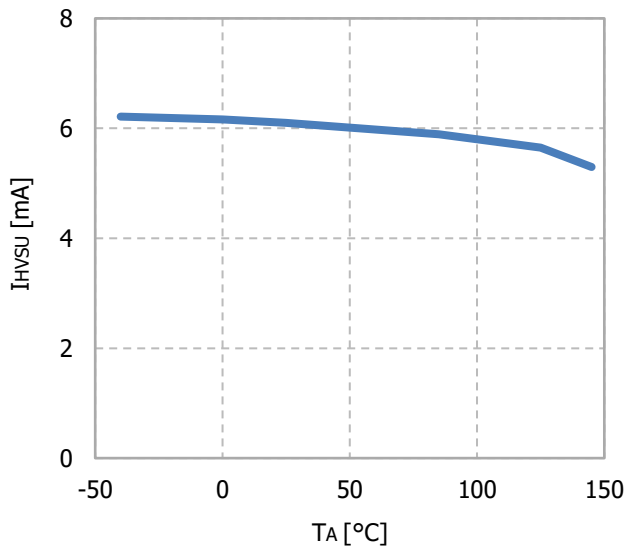


Typical Performance Characteristics

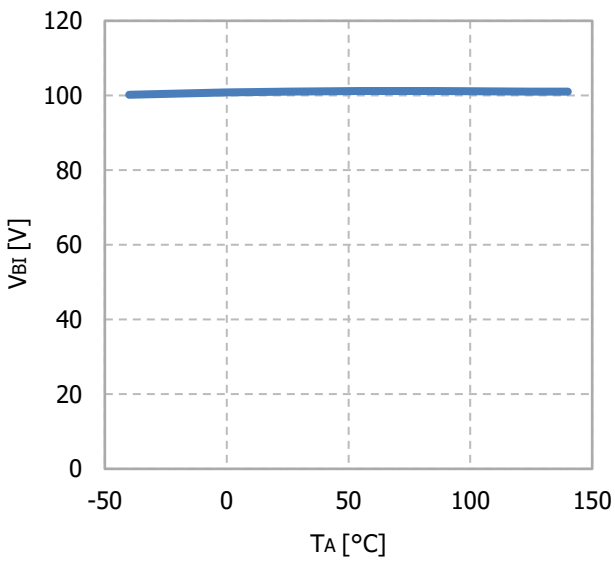
TA vs. HV Input Current



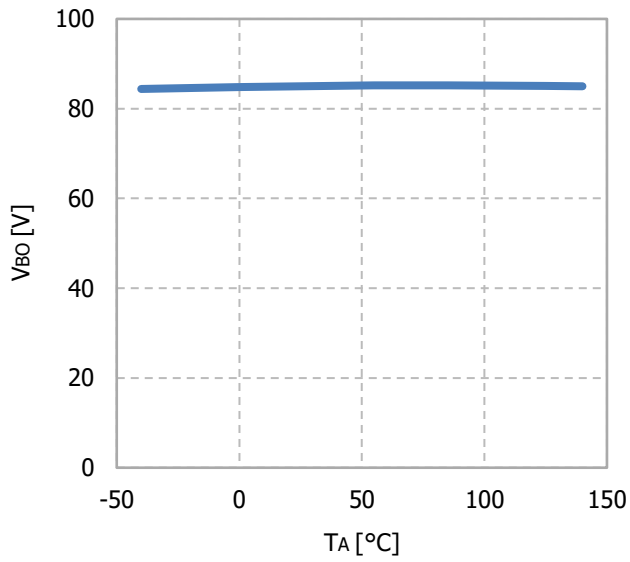
TA vs. Startup HV Input Current



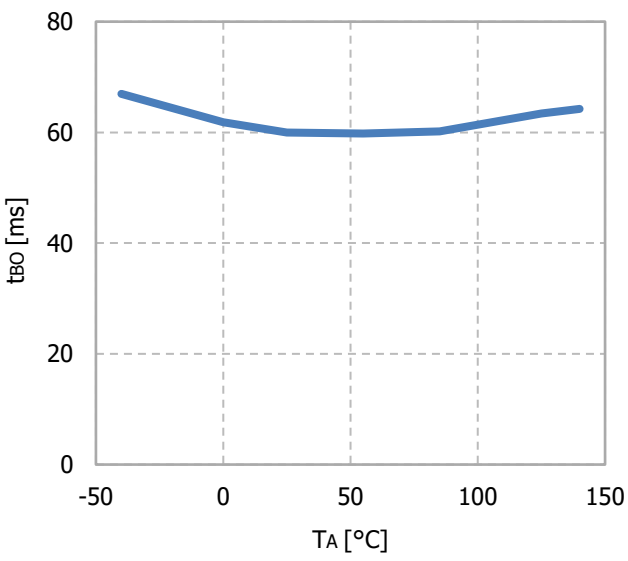
TA vs. Brown-In Voltage



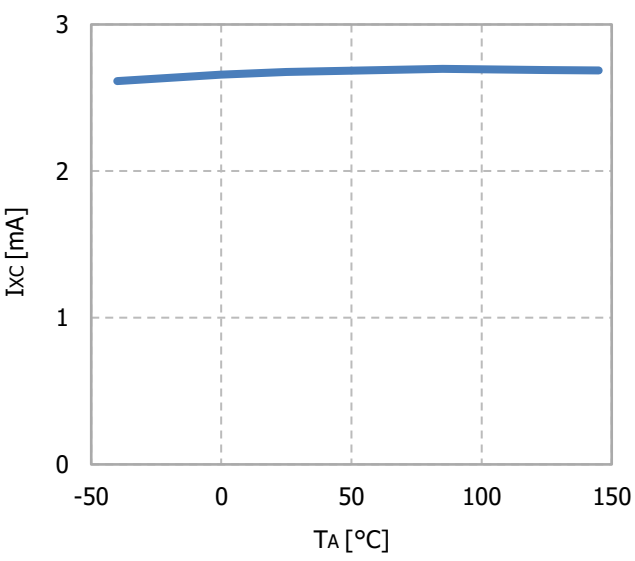
TA vs. Brown-Out Voltage



TA vs. Brown-Out Detection Delay Time

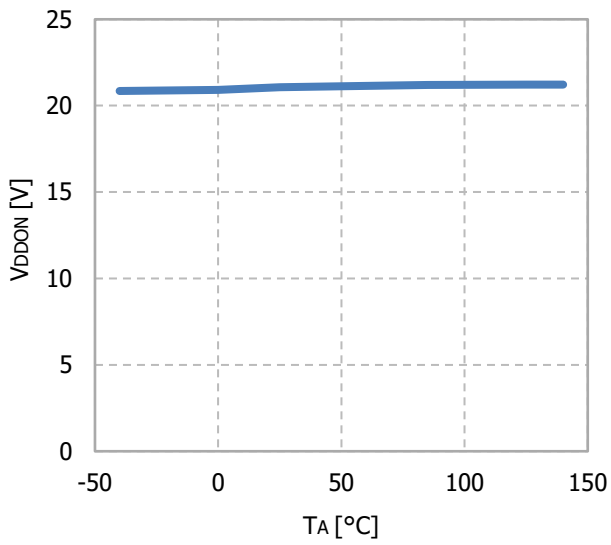


TA vs. X-Capacitor Discharge Current

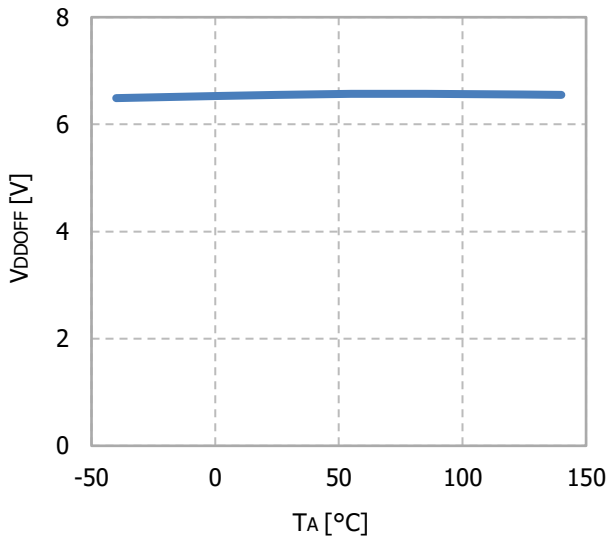


Typical Performance Characteristics

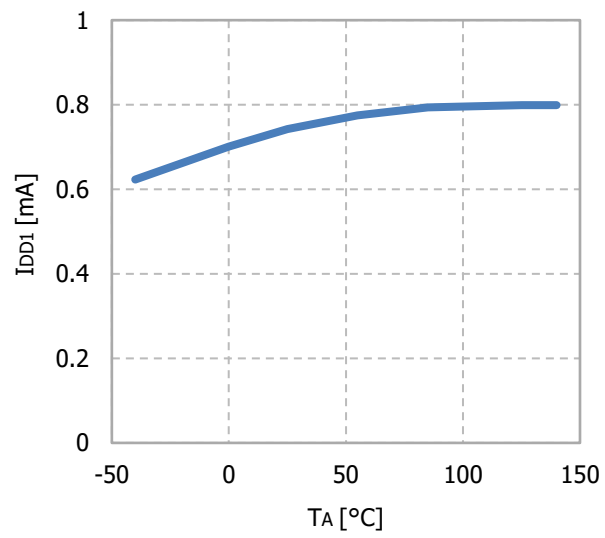
TA vs. Turn-On Operation Voltage



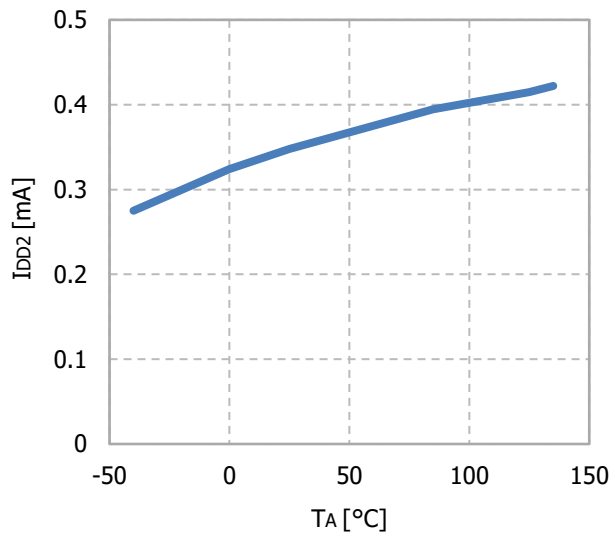
TA vs. Turn-Off Operation Voltage



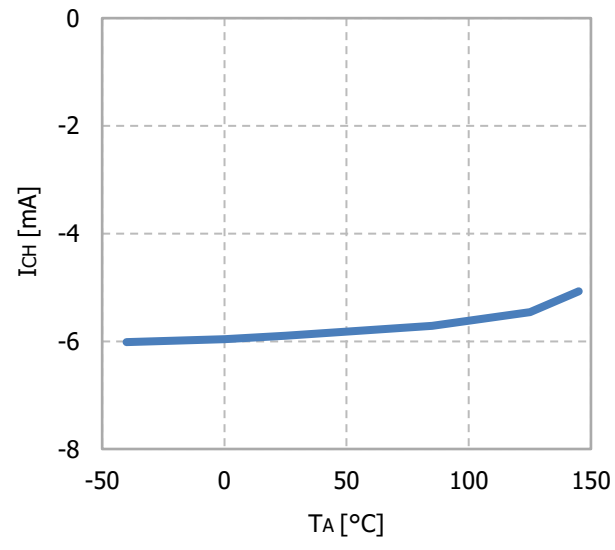
TA vs. Operating Current



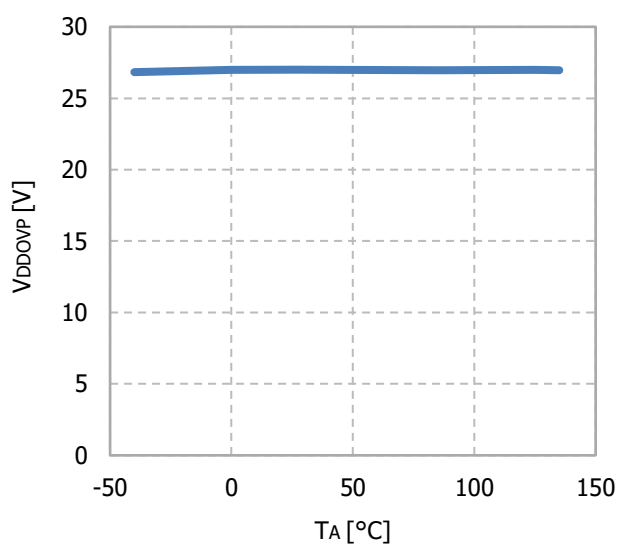
TA vs. Operating Current in No Switching



TA vs. Startup Charging Current

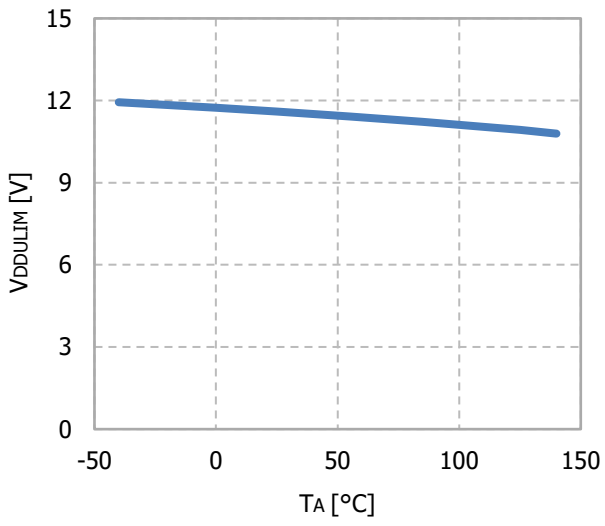


TA vs. VDD OVP Detection Voltage

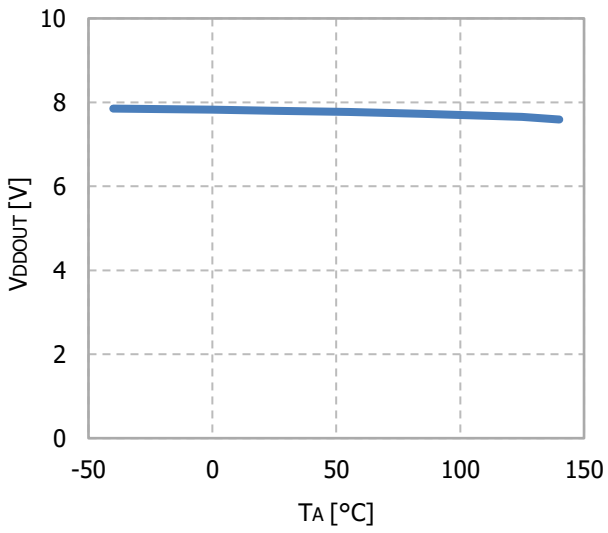


Typical Performance Characteristics

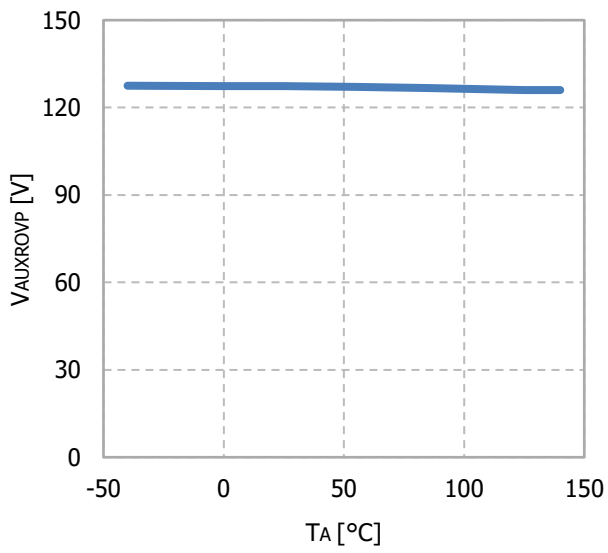
Built-in Regulator TA vs. VDD Clamped Output Voltage



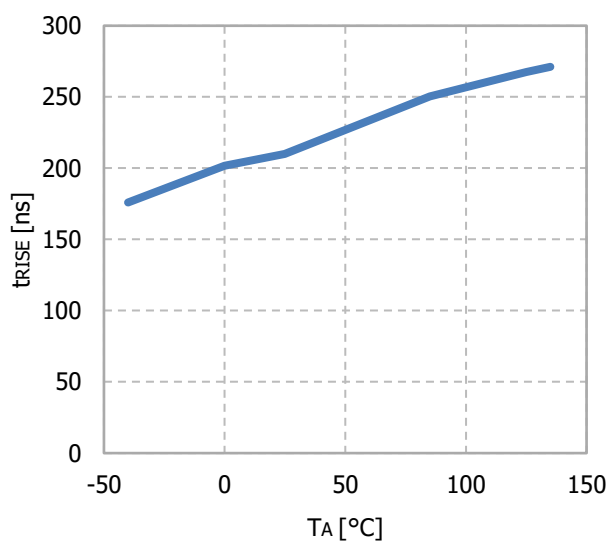
Built-in Regulator TA vs. VDD Output Voltage



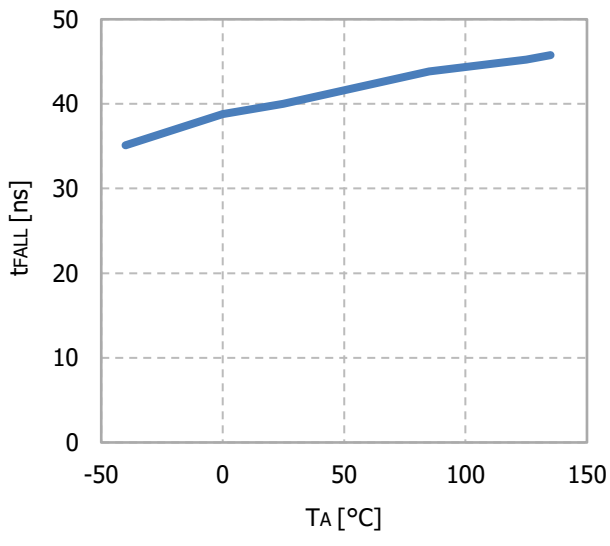
TA vs. AUXR OVP Detection Voltage



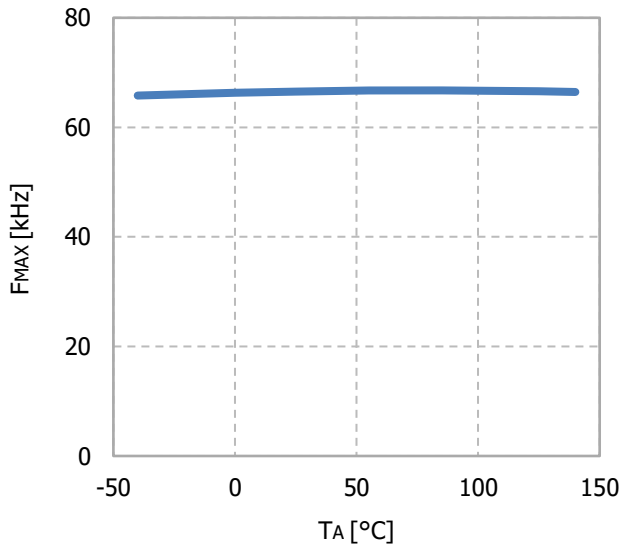
TA vs. Rise Time



TA vs. Fall Time

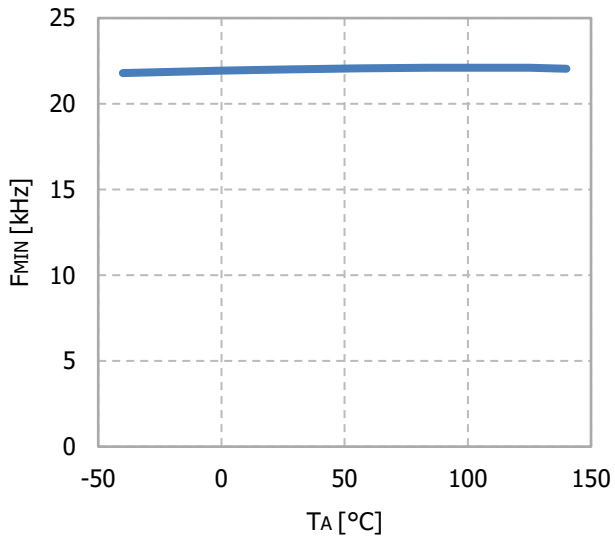


TA vs. Maximum Frequency

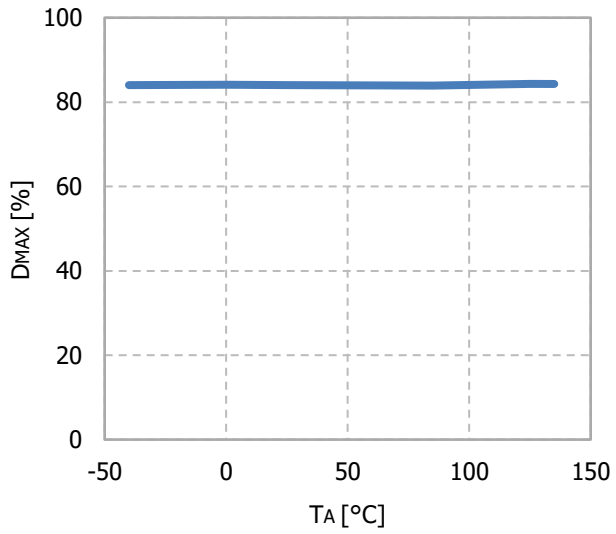


Typical Performance Characteristics

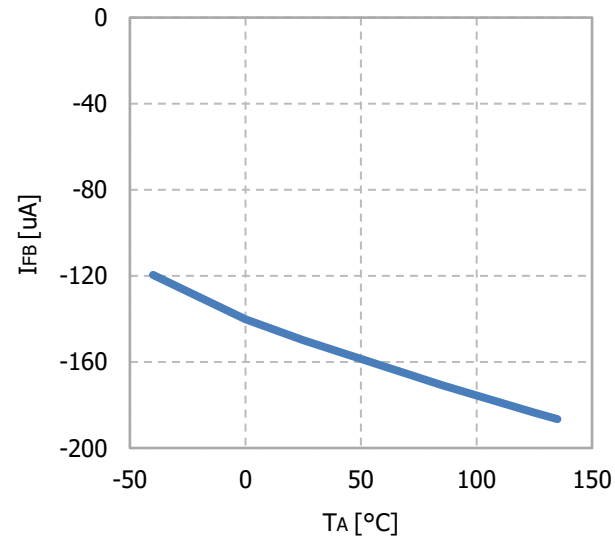
TA vs. Minimum Frequency



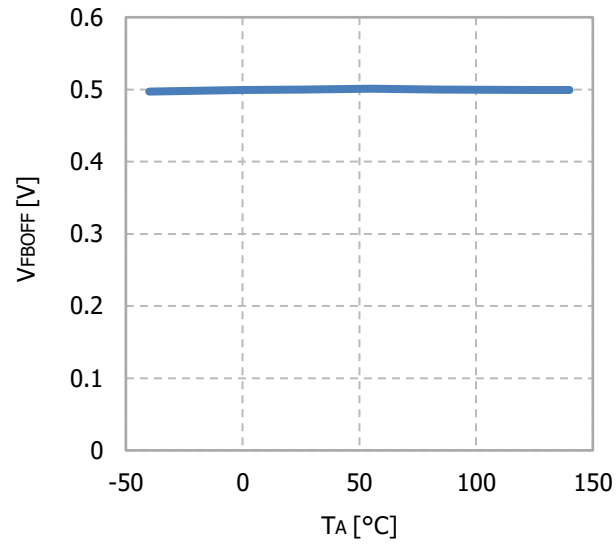
TA vs. Maximum On Duty Cycle



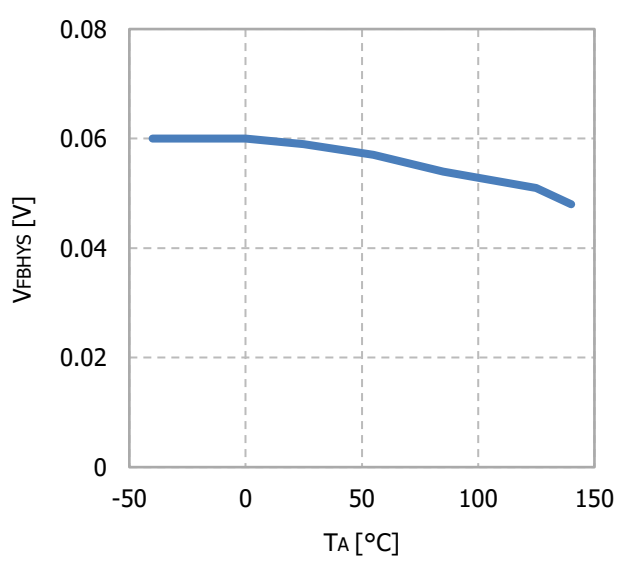
TA vs. FB Source Current



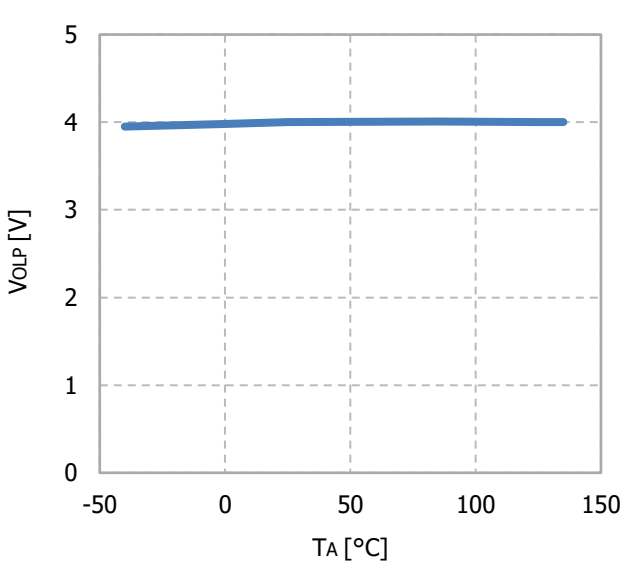
TA vs. Turn-Off Switching Voltage



TA vs. Turn-Off Switching Hysteresis Voltage

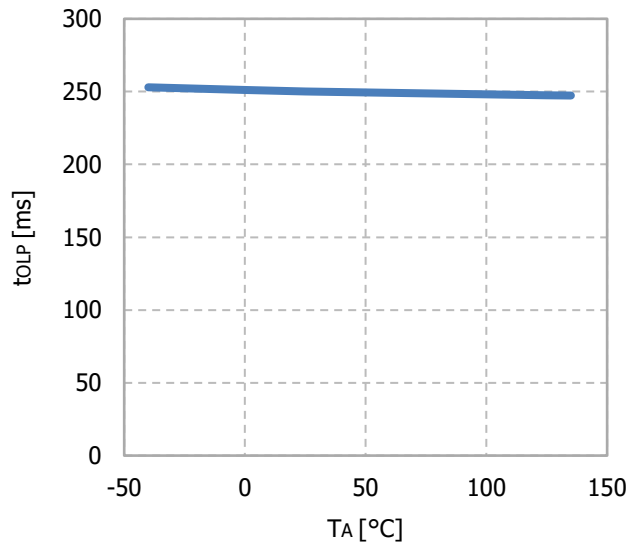


TA vs. OLP Detection Voltage

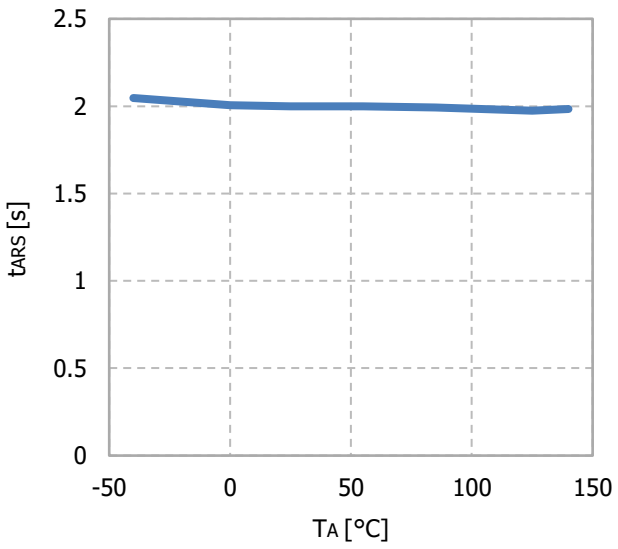


Typical Performance Characteristics

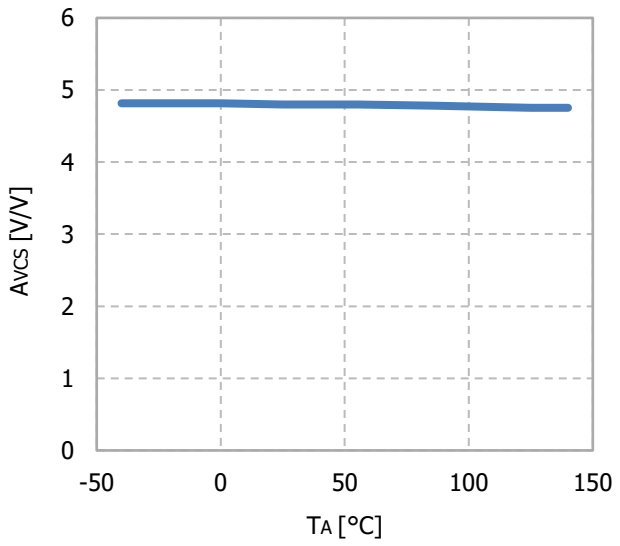
TA vs. OLP Delay Time



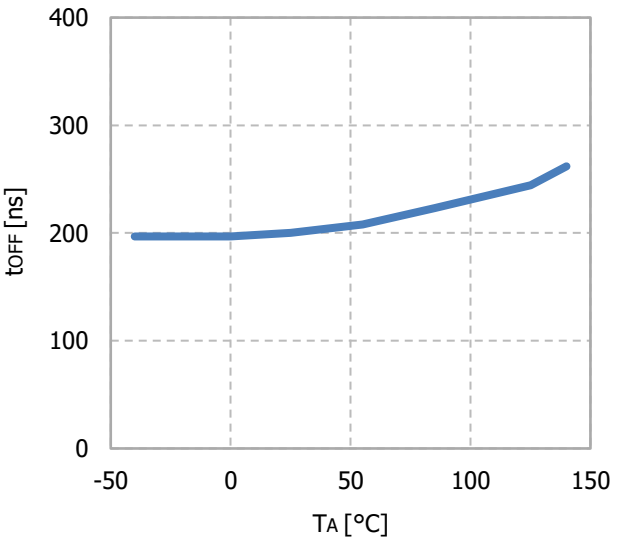
TA vs. Auto Restart Time



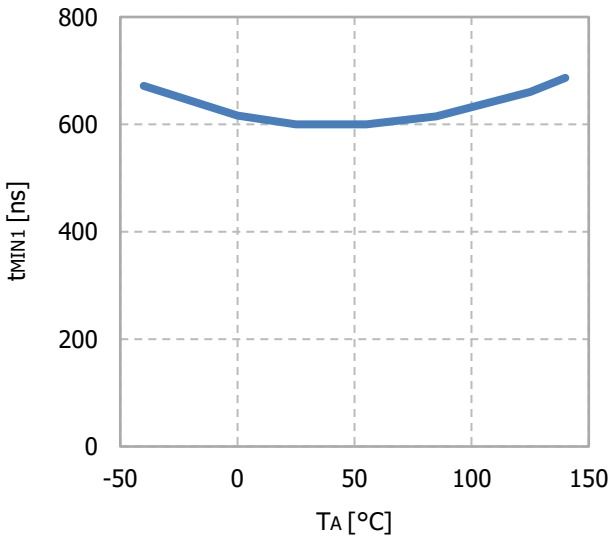
TA vs. Voltage Gain



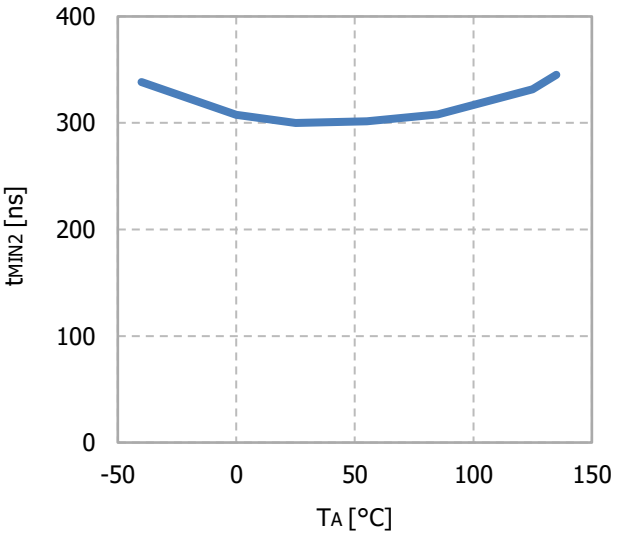
TA vs. GATE Turn-Off Delay Time



TA vs. Minimum On Time 1

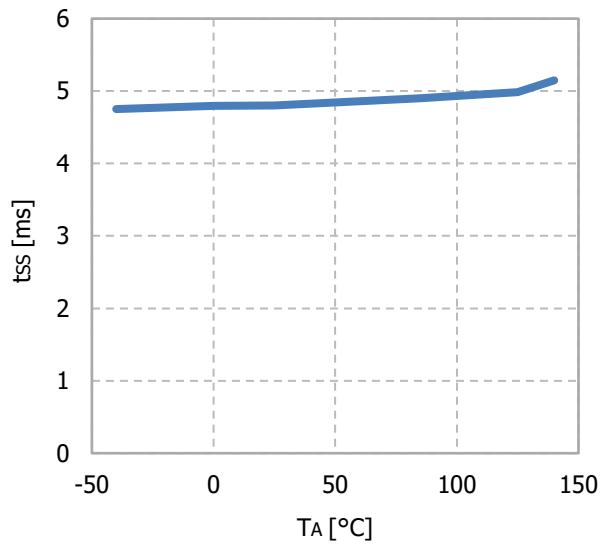


TA vs. Minimum On Time 2

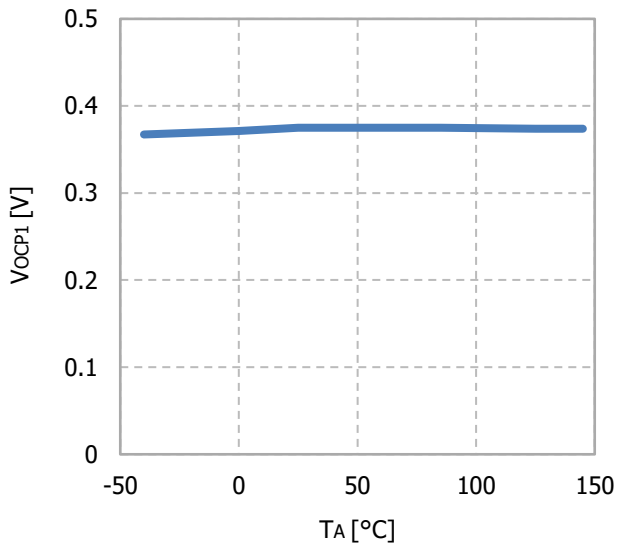


Typical Performance Characteristics

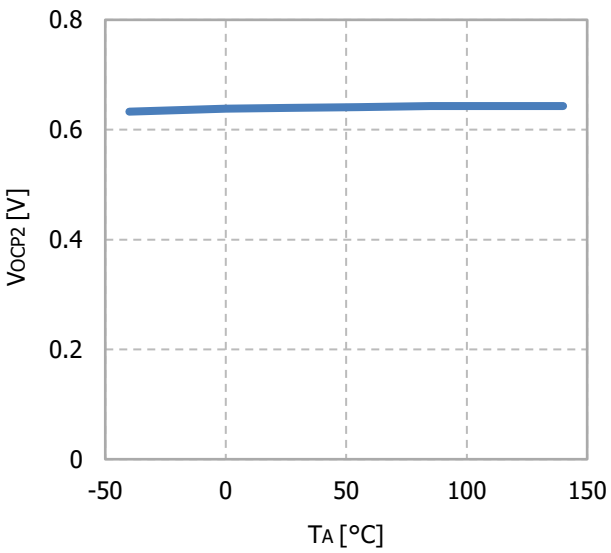
TA vs. Soft Start Time



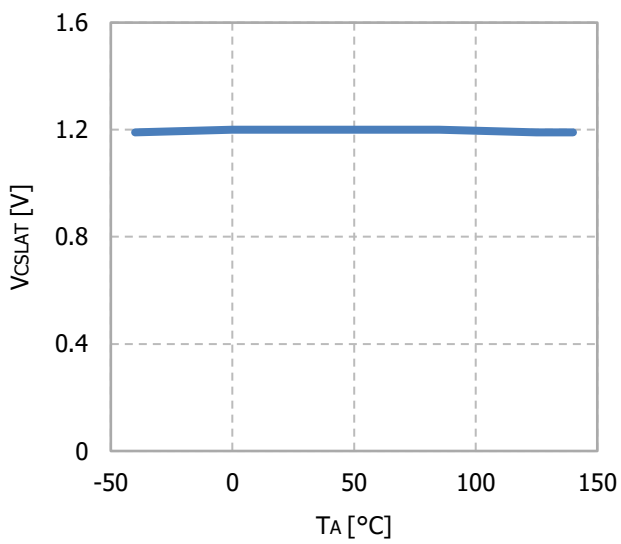
TA vs. OCP Detection Voltage 1



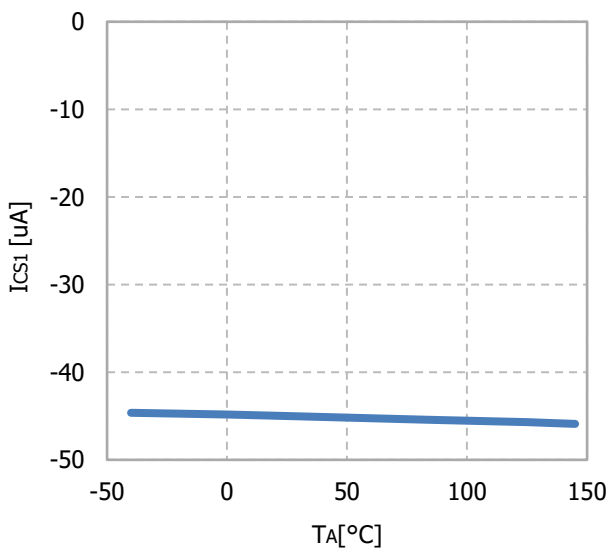
TA vs. OCP Detection Voltage 2



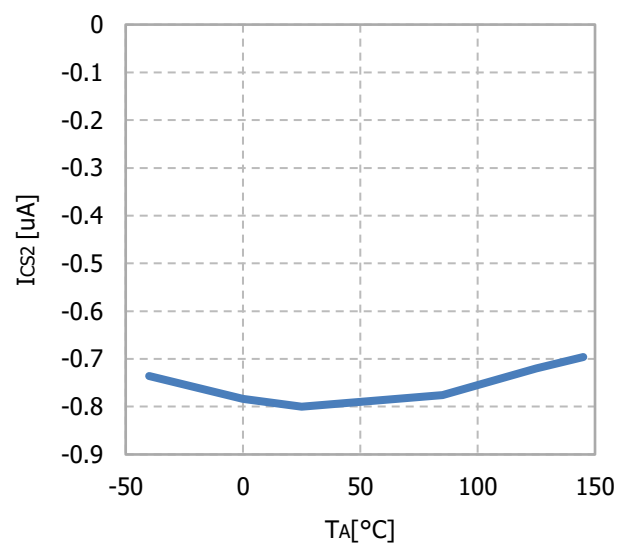
CS Latch-Off Detection Voltage



TA vs. CS Source Current 1

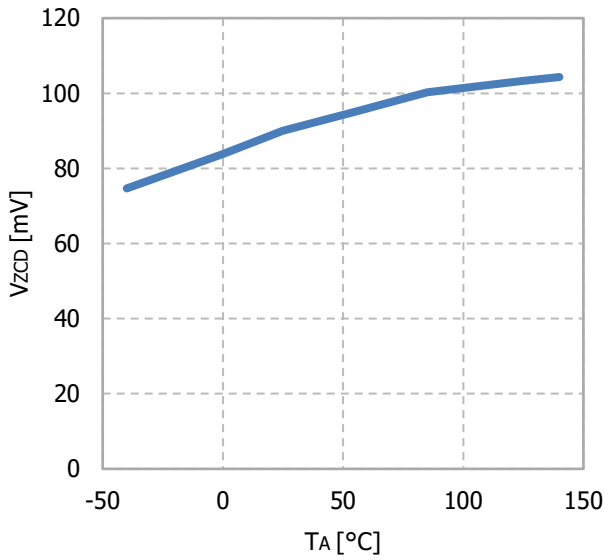


TA vs. CS Source Current 2

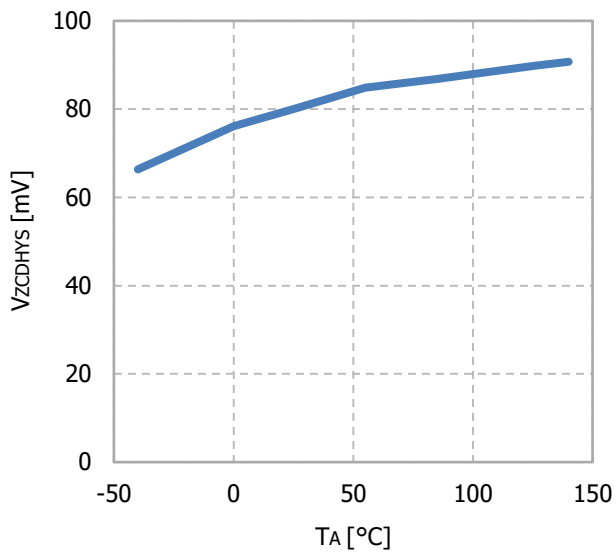


Typical Performance Characteristics

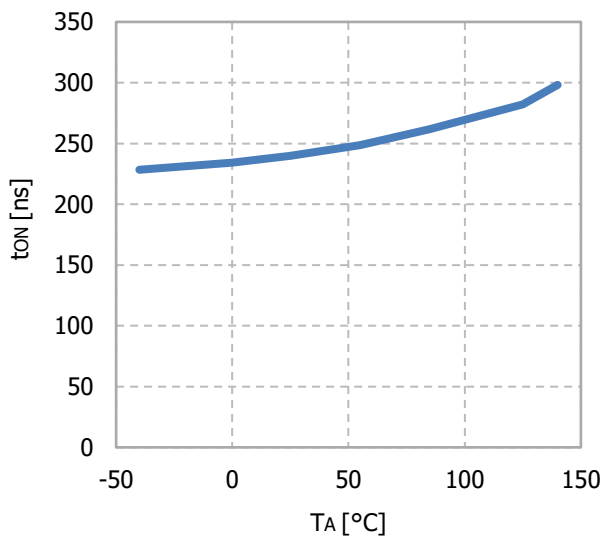
TA vs. Zero Current Detection (ZCD) Voltage



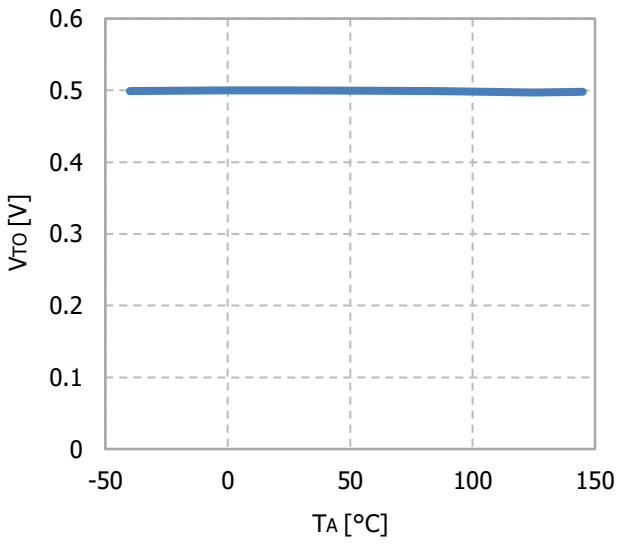
TA vs. ZCD Hysteresis Voltage



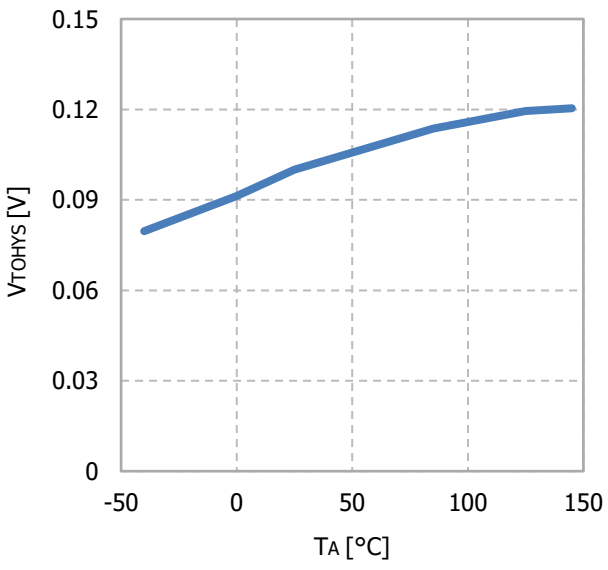
TA vs. GATE Turn-On Delay Time



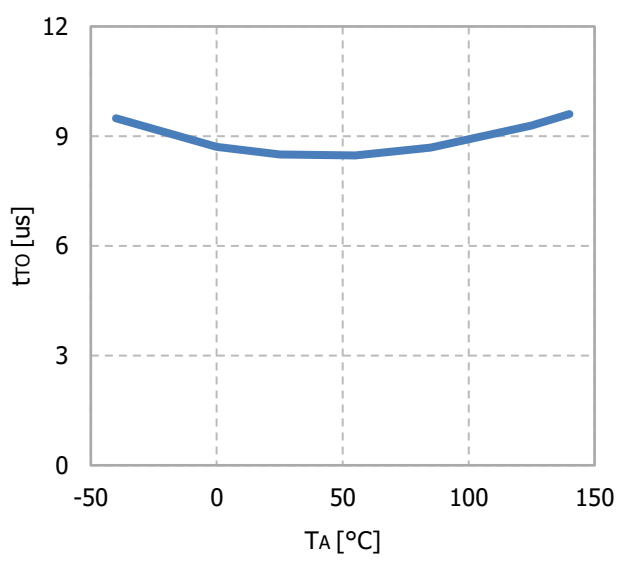
TA vs. ZCD Time-Out Entry Voltage



TA vs. ZCD Time-Out Hysteresis Voltage

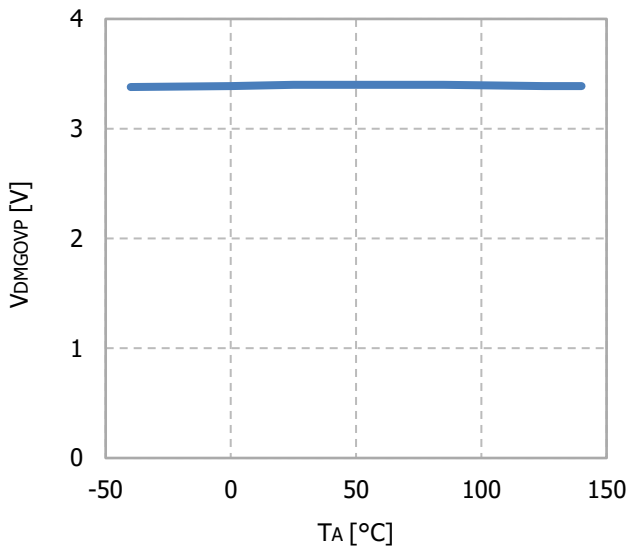


TA vs. ZCD Time-Out

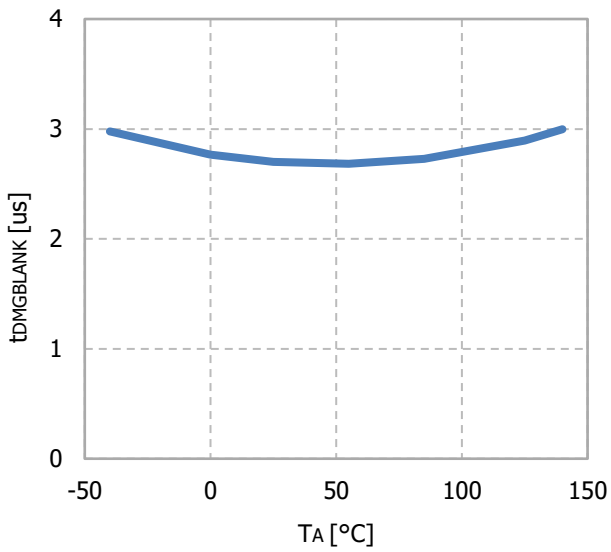


Typical Performance Characteristics

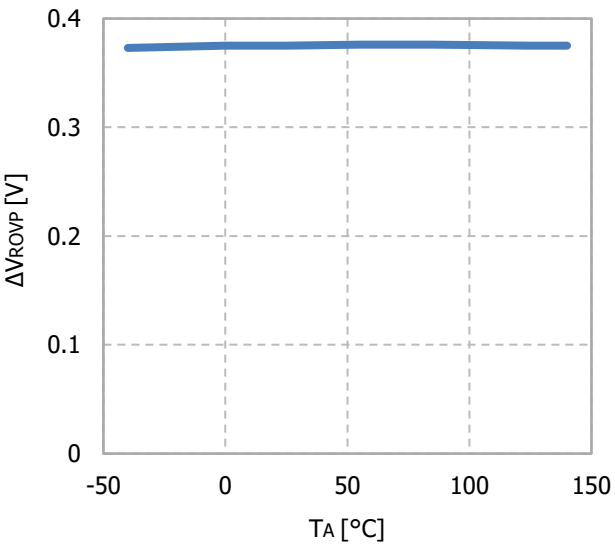
TA vs. DMG Constant OVP Detection Voltage



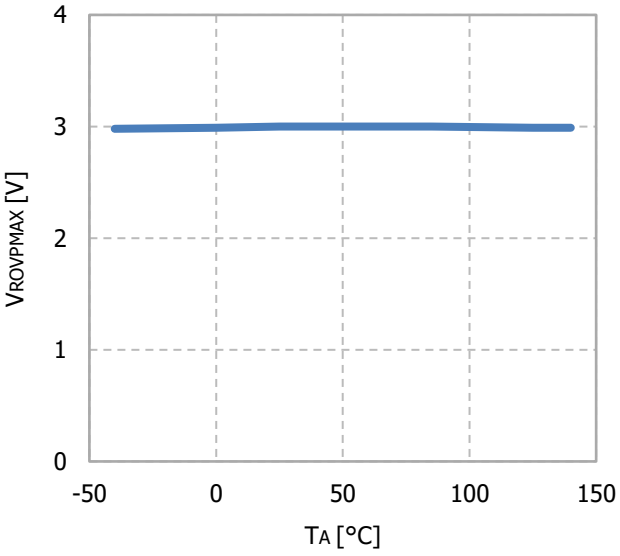
TA vs. DMG OVP Detection Blanking Time



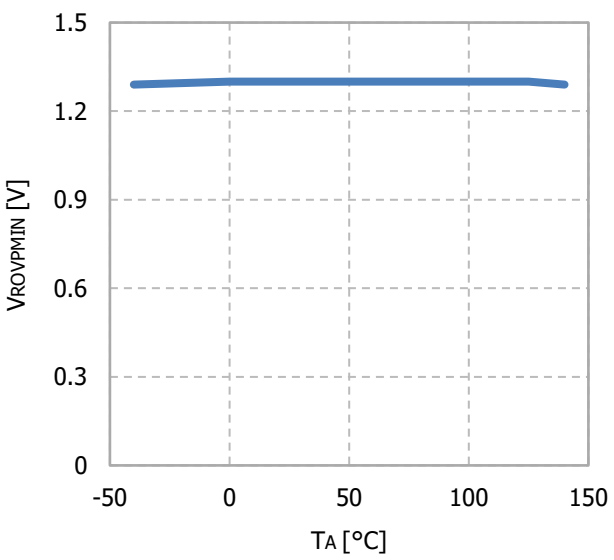
TA vs. DMG ROVP at Open Loop



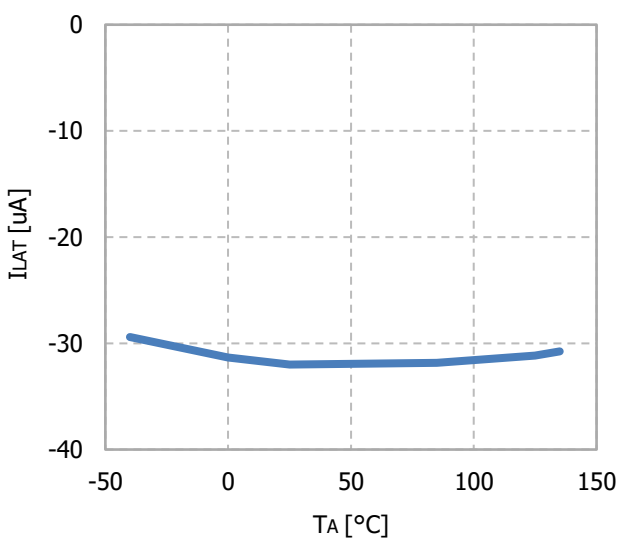
TA vs. DMG ROVP Upper Limit at Open Loop



TA vs. DMG ROVP Lower Limit at Open Loop

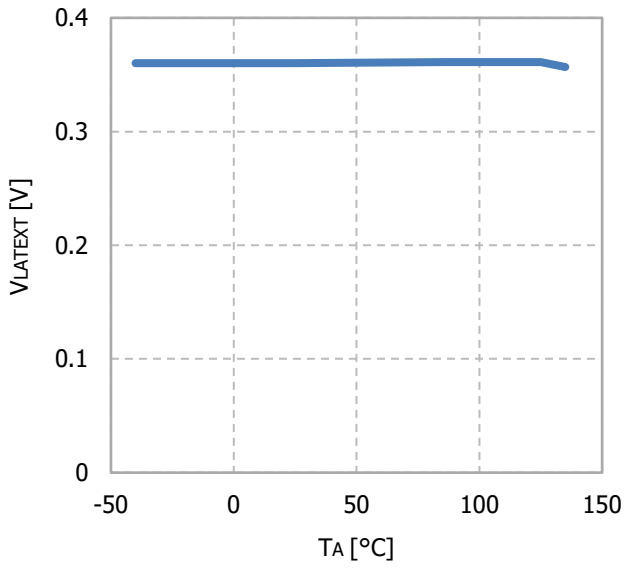


TA vs. LAT Source Current

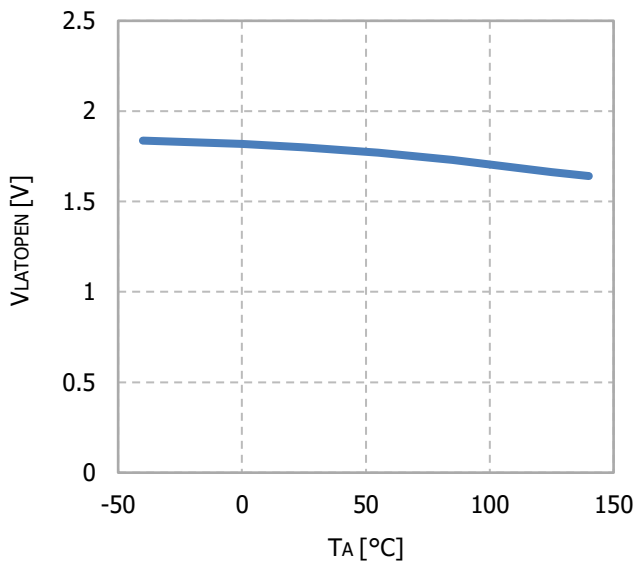


Typical Performance Characteristics

TA vs. External Latch-Off Voltage



TA vs. LAT Pin Open Voltage



Dimension

Package : SOP-10A

UNIT	mm

